Current Zero-Crossing Prediction Based Critical Conduction Mode Control of Totem-Pole PFC Rectifiers

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***Abstract*—Critical conduction mode (CRM) is widely used in totem-pole Boost power factor correction converters due to its compatibility with soft-switching and high switching frequency. Conventionally, a current sensor or zero-current detector is required to realize CRM operation. The system performances highly rely on the behaviors of peripheral circuits. Additional power loss and delay are also introduced. Moreover, the inductor current contains obvious differential mode noise, which brings interferences to the sensing signals. To address this issue, a novel CRM realization method is proposed. It utilizes an inductor current estimator model to estimate the averaged current and to predict the current zero-crossings. The noisy sensing signal is replaced by estimated values. Therefore, the zero-current detection circuit is removed, which simplifies the peripheral circuit design. Valley-switching and zero-voltage switching can also be achieved. Operation principles, digital implementation, and error suppression of the proposed control are analyzed. The proposed concepts are validated on a $550W$, $150\mathrm{k}Hz-1.6\mathrm{M}Hz$, GaN-based prototype. Experimental results record 98.96% peak efficiency with a 0.9972 power factor.**

***Index Terms*—Current zero-crossing prediction, critical conduction mode (CRM), power factor correction (PFC), totem-pole**

I. Introduction

Power factor correction (PFC) converters are widely used in applications such as telecommunication power supplies and battery chargers [1]. Boost and its derived topologies dominate in ac/dc PFC converters [2]. Among them, totem-pole Boost topology outperforms with low components count, simple structure, and bidirectional power flow [3]–[5].

In totem-pole Boost converters, continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CRM) are three major operation modes. Table I summarizes the features of CCM, DCM, and CRM. As indicated, CCM provides low conduction loss but suffers from severe diode reverse recovery and high MOSFET turning-on loss. DCM mitigates the diode reverse recovery by zero-current-switching (ZCS) with simple structure and control [6]. However, the power rating is limited. It is preferred to be used at light load when the conduction loss is non-dominant. In comparison, CRM facilitates the MOSFET zero-voltage-switching (ZVS) or valley-switching turning-on using quasi-resonant technique [7]. At higher power levels, CRM is preferred to DCM as its backflow current is negligible [8], [9]. Therefore, CRM is considered the optimal solution in medium power applications.

TABLE I
Comparison of CCM, DCM, and CRM

Mode	Current stress	Soft switching	Power level
CCM	Low	no	High
DCM	High	ZCS-on	Low
CRM	Medium	Valley-switching/ ZVS-on	Medium

In CRM operation of totem-pole Boost converters, zero-current detection (ZCD) circuit is widely employed [10]–[14]. ZCD circuit locates the inductor current zero-crossings when the switching loss is minimum [10], [11]. As a standing point, many derivative works are investigated to improve the power factor and efficiency performances. In [12], two phases are interleaved to mitigate the input filter attenuation requirement. In [13], by controlling the on-time of the switch in the synchronous rectifier (SR), predictive ZVS and limited switching frequency can be realized. In [14], harmonic injection is utilized to optimize the switching frequency range. A ZCD signal is generated by comparing a current sensing signal with zero. However, few low-cost hall current sensors are available beyond hundreds of $\mathrm{k}Hz$.

At high frequencies, current shunts and transformers are commonly used. Current shunt solutions have the advantage of high current sensing bandwidth [10]–[13]. However, the inductor current shape tends to be distorted by the resistive shunt. This leads to a degraded total harmonic distortion (THD). In [15], Shahzad et al. adopt a small sensing resistor to reduce the negative effect and utilize an op-amp to amplify the current signal, which requires additional components. In [16], the current loop is compensated for the resistive part in the plant model of the converter. Meanwhile, to improve the sensing signal immunity, a hysteretic comparative window is introduced and generates a time delay between the ZCD

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signal and the current zero-crossing point, which affects the performance [17]. In [18], an auxiliary winding is coupled with the boost inductor. ZCD signal is captured when the boost inductor's voltage commutates to positive. In [19], the maximum voltage drop on the secondary windings is limited by a saturable core. The conduction loss is reduced compared with the shunt solutions. However, the transformer cores are bulky and the time delay of ZCD still exists.

To overcome the limitations of the ZCD circuits, ZVS-catch methods are developed in [20], [21]. It directly senses the drain-source voltage and detects its zero-crossing point. However, this method is demanding in the circuit design due to the switching noise from the drain-source voltage. In [20], this method is first applied with on-chip design. In [21], the board stage realization is achieved with a novel diode-clamped circuit.

Increasing the current ripple on the CCM designs can also achieve CRM operation [22]–[25]. In [22], a high-speed current sensor is utilized in the feedback loop and the inductor current ripple is directly controlled. In [23]–[25], frequency modulation method is used to inject a programmed current ripple into the boost inductor current. The performance of these methods relies on the current loop. However, large differential mode noise exists on the inductor current sensing signals [26]. This mainly attributes to the CRM operation. The frequency response of the current sensor also introduces additional phase offsets at high frequencies.

To avoid the usage of inaccurate current sensing signals, many predictive current sensorless control methods are developed for PFC converters [27]–[29]. Accordingly, the advantages of CRM over CCM in terms of high conversion efficiency and simple control are further highlighted. However, removing both the current sensor and the ZCD/ZVS catch circuit makes the control more challenging. Moreover, these reported methods mainly focus on CCM control under small current ripple assumptions. In CRM scenarios, large current ripples deteriorate the accuracy of the averaged inductor current model.

In this manuscript, a current zero-crossing prediction-based CRM control is proposed for the totem-pole PFC rectifier. The major research contributions include:

1) A novel current estimator is proposed for CRM control. The behaviors of the estimator considering the nonlinear output capacitance of switching devices are modeled and analyzed.

2) The proposed current estimator predicts the inductor's current zero-crossing points. Thus, conventional ZCD circuit is removed. This reduces the component count of the peripheral circuits and the resistive losses in the power circuit. Moreover, to improve the prediction performance, a disturbance damping control is proposed to mitigate the variation of inductance and parasitic resistance.

4) Conventional double-loop control scheme is simplified. The proposed current estimator provides information on both the instant current and average current. The noisy CRM current signal is excluded from the control loop.

5) High power factor and high efficiency can be realized simultaneously. No current sensor, ZCD circuit, or ZVS-catch circuits are required. Valley-switching and zero-voltage switching are achieved.

6) The proposed concept is naturally compatible with high-frequency GaN devices.

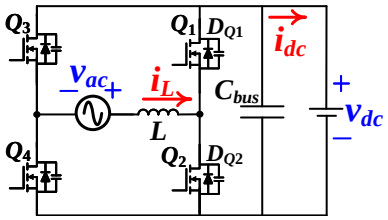


Fig. 1. Schematic of the totem pole Boost PFC converter.

The manuscript is organized as follows. Section II introduces the operating principles of CRM totem-pole converter. The proposed current estimator with zero-current prediction is derived in Section III. The proposed estimator-based CRM control is detailed in Section IV. In Section V, experimental results are demonstrated. Section VI concludes this article.

II. Steady State Analysis of CRM Operation

A typical single-phase totem-pole Boost PFC rectifier is illustrated in Fig. 1. It contains two high-frequency switches Q_1, Q_2, two low-frequency switches Q_3, Q_4, and a Boost inductor L. D_{Q1} and D_{Q2} are body diodes of Q_1 and Q_2, respectively. i_L is the current of L. v_{ac} is the input ac voltage. C_{bus} is the filtering capacitor on the dc-link. v_{dc} is the dc-link voltage.

The positive half-cycle can be divided into seven operation states as shown in Fig. 2. The negative half-cycle is similar. Since the switching frequency is much higher than line frequency, v_{dc}, v_{ac} can be considered as constants over one specific switching cycle.

According to whether D_{Q1} conducts, the circuit operation can be divided into two categories, as shown in Fig. 3 and Fig. 4. In the normal power transfer scenario, D_{Q1} conducts. Once D_{Q1} conducts, there's a positive power flowing into the dc-link. In the non-power transfer scenario, only circulating power exists.

A. Normal Power Transfer Scenarios

Typical waveforms of the normal power transfer scenario are shown in Fig. 3. t_0, t_4, and t_7 are current zero-crossing instants.

a) State I*: t_0–t_1:* During this time interval, the circuit is in State I. The voltage across L is v_{ac}. i_L increases linearly as,

$$i_L = \frac{v_{ac}}{L}(t - t_0) \tag{1}$$

b) State II*: t_1–t_2:* The circuit is in State II. C_{oss} of Q_1 and Q_2 resonates with L. When D_{Q1} conducts at t_2, this state ends. The ZVS condition for Q_1 is created. The characteristic impedance (Z_n) and resonant frequency (ω_n) are,

$$Z_n = \sqrt{\frac{L}{2C_{oss}}}, \omega_n = \frac{1}{\sqrt{2C_{oss}L}}$$

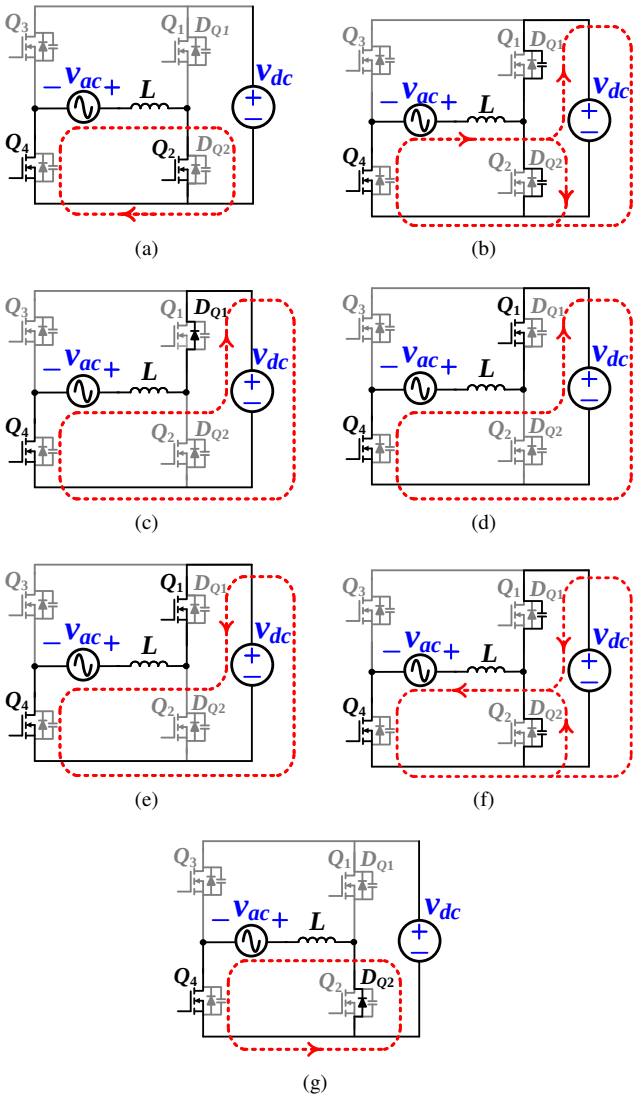


Fig. 2. Operation states in positive half line cycle (a) State I, (b) State II, (c) State III, (d) State IV, (e) State V, (f) State VI, (g) State VII.

Drain-source voltage of Q_2 ($v_{ds,Q2}$) and i_L yield to the second-order transient response.

$$\begin{aligned} v_{ds,Q2} =& v_{ac} + Z_n i_L(t_1)\sin\left[\omega_n(t-t_1)\right] \\ & - v_{ac}\cos\left[\omega_n(t-t_1)\right] \end{aligned} \tag{2}$$

$$i_L = \frac{v_{ac}}{Z_n}\sin\left[\omega_n(t-t_1)\right] + i_L(t_1)\cos\left[\omega_n(t-t_1)\right] \tag{3}$$

c) State III*:* t_2–t_3*:* During this time interval, the circuit is in State III. D_{Q1} conducts with a voltage drop V_D. This state ends when the gate signal of Q_1 rises. i_L linearly decreases as,

$$i_L = i_L(t_2) + \frac{v_{ac} - v_{dc} - V_D}{L}(t-t_2) \tag{4}$$

d) State IV*:* t_3–t_4*:* When SR is enabled at t_3, the circuit enters into State IV. Q_1 is turned on such that i_L flows through the MOSFET channel. i_L decreases linearly. At t_4, i_L crosses zero.

$$i_L = i_L(t_3) + \frac{v_{ac} - v_{dc}}{L}(t-t_3) \tag{5}$$

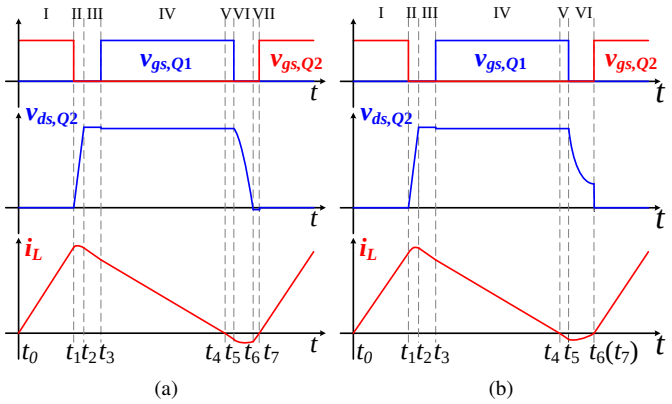


Fig. 3. Typical waveforms of gate signals, drain-source voltage, and the inductor current in CRM operation for normal power transfer scenarios: (a) ZVS case and (b) valley-switching case.

e) State V*:* t_4–t_5*:* During this time interval, the circuit is in State V. i_L flows back to the source v_{ac}. This state ends at t_5 when the gate signal of Q_1 changes to zero.

$$i_L = \frac{v_{ac} - v_{dc}}{L}(t-t_4) \tag{6}$$

f) State VI*:* t_5–t_6*:* C_{oss} resonates with L in State VI. At t_6, $v_{ds,Q2}$ reaches its valley, which creates a ZVS or valley-switching condition for Q_2. In ZVS conditions, this state ends at t_6, as shown in Fig. 3 (a). For some scenarios, $v_{ds,Q2}$ never hits zero. Then this state ends at t_7, which corresponds to the valley point, as demonstrated in Fig. 3 (b). $v_{ds,Q1}$ and i_L yield,

$$\begin{aligned} v_{ds,Q1} =& v_{dc} - v_{ac} - (v_{dc} - v_{ac})\cos\left[\omega_n(t-t_5)\right] \\ & - Z_n i_L(t_5)\sin\left[\omega_n(t-t_5)\right] \end{aligned} \tag{7}$$

$$i_L = \frac{v_{ac} - v_{dc}}{Z_n}\sin\left[\omega_n(t-t_5)\right] + i_L(t_5)\cos\left[\omega_n(t-t_5)\right] \tag{8}$$

ZVS of Q_2 can be realized if $v_{ac} \le 0.5 v_{dc}$. Otherwise the ZVS condition depends on $i_L(t_5)$. If $i_L(t_5)$ is close to zero, valley-switching is realized, $t_6 = t_7$.

The differences between states II and VI mainly lie in the initial condition and ZVS or valley-switching energy source. In State II, the ZVS energy comes from the ac source. While in State VI, the ZVS or valley-switching energy comes from the dc-link.

g) State VII*:* t_6–t_7*:* During this period, i_L increases linearly. The circuit is in State VII. D_{Q2} conducts. This state ends at t_7 when i_L hits zero. Another switching cycle starts at t_7. i_L is,

$$i_L = i_L(t_6) + \frac{v_{ac} + V_D}{L}(t-t_6) \tag{9}$$

B. Nonpower Transfer Scenarios

In some scenarios, the peak i_L is insufficient to fully charge the C_{oss} of Q_1. Therefore $v_{ds,Q1}$ never falls below zero. Hence, Q_1 is kept off. Then, states III, IV, and V do not exist. The converter works in nonpower transfer scenarios. Typical waveforms in the nonpower transfer scenarios are demonstrated in Fig. 4.

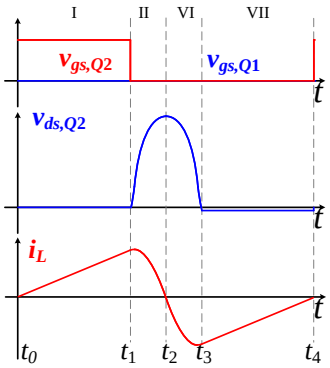


Fig. 4. Typical gate signals, drain-source voltage, and the inductor current in CRM operation for nonpower transfer scenarios.

a) State I*:* t_0–t_1*:* The circuit is in State I. i_L linearly increases. The state ends at t_1. i_L is as follows.

$$i_L = \frac{v_{ac}}{L}(t - t_0) \tag{10}$$

b) State II*:* t_1–t_2*:* The circuit is in State II. C_{oss} of Q_1 and Q_2 resonates with L. This state ends when i_L crosses zero at t_2. $v_{ds,Q2}$ and i_L are derived,

$$\begin{aligned} v_{ds,Q2} =& v_{ac} + Z_n i_L(t_1)\sin\left[\omega_n(t-t_1)\right] \\ & - v_{ac}\cos\left[\omega_n(t-t_1)\right] \end{aligned} \tag{11}$$

$$i_L = \frac{v_{ac}}{Z_n}\sin\left[\omega_n(t-t_1)\right] + i_L(t_1)\cos\left[\omega_n(t-t_1)\right] \tag{12}$$

c) State VI*:* t_2–t_3*:* The circuit is in State VI. C_{oss} of Q_1 and Q_2 resonates with L. This state ends when D_{Q2} conducts at t_3. $v_{ds,Q2}$ and i_L are derived,

$$\begin{aligned} v_{ds,Q2} =& v_{ac} + v_{ac}\sin\left[\omega_n(t-t_2) + \arctan\frac{v_{ac}}{Z_n i_L(t_1)}\right] \\ & + Z_n i_L(t_1)\cos\left[\omega_n(t-t_2) + \arctan\frac{v_{ac}}{Z_n i_L(t_1)}\right] \end{aligned} \tag{13}$$

$$\begin{aligned} i_L =& \frac{v_{ac}}{Z_n}\cos\left[\omega_n(t-t_2) + \arctan\frac{v_{ac}}{Z_n i_L(t_1)}\right] \\ & - i_L(t_1)\sin\left[\omega_n(t-t_2) + \arctan\frac{v_{ac}}{Z_n i_L(t_1)}\right] \end{aligned} \tag{14}$$

In State II, VI of nonpower transfer scenario, the time interval $t_3 - t_1$ is longer than half the resonant period, $t_3 - t_1 = [\pi + 2\arctan(v_{ac}/i_L(t_1)/Z_n)]/\omega_n$.

d) State VII*:* t_3–t_4*:* The circuit is in State VII. During this time interval, i_L increases linearly. D_{Q2} conducts. This state ends at t_4 when i_L hits zero. Another switching cycle starts at t_4. i_L is expressed as,

$$i_L = i_L(t_4) + \frac{v_{ac} + V_D}{L}(t - t_6) \tag{15}$$

III. Proposed Current Estimator Model

To avoid the limitations of current sensors and ZCD circuits in CRM control, an accurate current estimator model is required to predict the current zero-crossing points. In CRM, the current ripple is high and resonance may occur in the deadband. This brings challenges to the modeling of current estimator. In [30], C_{oss} is modeled as a time-related capacitor to calculate i_L in (3) and (8). The model has satisfied accuracy in estimating the ZVS or valley-switching time and the peaks or valleys of the current during the resonance. However, C_{oss} exhibits high nonlinearity and brings errors to the current estimation and zero-crossing prediction [31]. To cope with this issue, we propose a novel current estimator model. In this model, the charge exchanged during the deadband is utilized to estimate i_L, and the time-related capacitor is utilized to calculate ZVS or valley-switching condition.

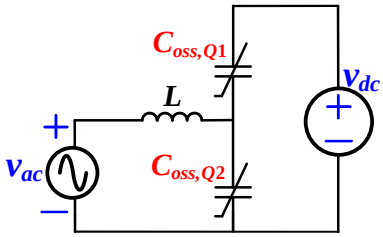


Fig. 5. Equivalent resonant circuit in the deadband with nonlinear capacitance of Q_1 and Q_2.

A. Deadband Resonance Analysis

The accuracy of the current estimator affects the PFC performance. Behaviors of the estimator imitate the i_L model. Nonlinear C_{oss} makes the conventional model inaccurate for i_L estimation in the deadband. Therefore, the deadband resonance considering the nonlinearity is investigated in this section, as illustrated in Fig. 5.

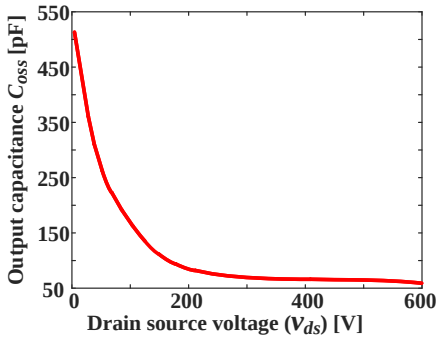
In non-power transfer case, the symmetrical characteristics of i_L in the deadband have been analyzed in the previous section. Therefore, this section focuses on the analysis of i_L during normal power transmission. The following model takes into account the nonlinear characteristics of C_{oss}, as shown in Fig. 6. C_{oss} in Fig. 6 (a) is extracted from the datasheet. The stored charge in Fig. 6 (b) is obtained by integrating C_{oss} over v_{ds}. Fig. 6 (c) shows the sum of $E_{oss,Q1}$ and $E_{oss,Q2}$, where E_{oss} is stored energy in the corresponding transistor.

a) State II $t_1 \sim t_2$*:* In State II, $C_{oss,Q2}$ is charged and $C_{oss,Q1}$ is discharged. $Q_{top,f}$ and $Q_{bot,f}$ are noted as the charge exchanged in Q_1 and Q_2 during this process respectively.

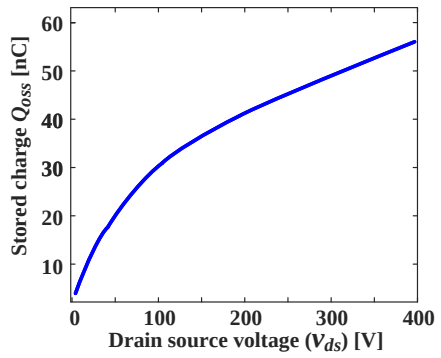
$$\begin{aligned} Q_{top,f} =& -\int_{t_1}^{t} i_{ds,Q1}dt \\ =& Q_{oss}(v_{dc}) - Q_{oss}(v_{dc} - v_{ds,Q2}(t)) \\ Q_{bot,f} =& \int_{t_1}^{t} i_{ds,Q2}dt = Q_{oss}(v_{ds,Q2}(t)) \end{aligned} \tag{16}$$

According to energy conservation,

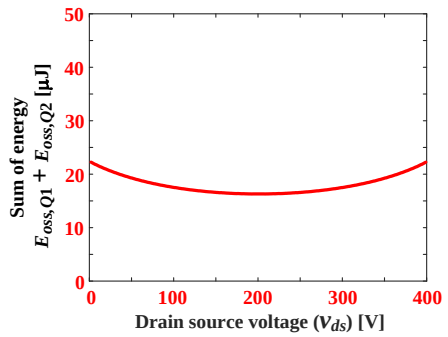
$$\begin{aligned} & \frac{1}{2}Li_L^2(t_1) + (Q_{top,f} + Q_{bot,f})v_{ac} + E_{oss,Q1}(t_1) + E_{oss,Q2}(t_1) \\ & = \frac{1}{2}Li_L^2(t) + v_{dc}Q_{top,f} + E_{oss,Q1}(t) + E_{oss,Q2}(t) \end{aligned} \tag{17}$$



(a)



(b)



(c)

Fig. 6. Relationship between drain-source voltage $v_{ds,Q2}$ and (a) C_{oss} (b) Q_{oss} (c) sum of output capacitance energy $E_{oss,Q1} + E_{oss,Q2}$.

At t_1, $v_{ds,Q2} = 0$. At t_2, $v_{ds,Q2} = v_{dc}$. According to Fig. 6 (c), $E_{oss,Q1}(t_1) + E_{oss,Q2}(t_1) = E_{oss,Q1}(t_2) + E_{oss,Q2}(t_2)$. Hence, the equation can be rewritten as (18).

$$\begin{aligned} &\frac{1}{2}Li_L^2(t_1) + [Q_{top,f}(t_2) + Q_{bot,f}(t_2)]v_{ac} \\ &= \frac{1}{2}Li_L^2(t_2) + v_{dc}Q_{top,f}(t_2) \end{aligned} \tag{18}$$

At t_2, i_L is derived as,

$$\begin{aligned} &i_L(t_2) \\ &= \sqrt{i_L(t_1)^2 + \frac{2}{L}\left[Q_{top,f}(t_2)(v_{ac} - v_{dc}) + Q_{bot,f}(t_2)v_{ac}\right]} \end{aligned} \tag{19}$$

b) State VI $t_5 \sim t_6$: In State VI, $C_{oss,Q1}$ is charged and $C_{oss,Q2}$ is discharged. $Q_{top,r}$ and $Q_{bot,r}$ are noted as the charge exchanged in Q_1 and Q_2 during this process respectively.

$$\begin{aligned} Q_{top,r} &= -\int_{t_5}^{t} i_{ds,Q1}dt \\ &= -Q_{oss}(v_{dc} - v_{ds,Q2}(t)) \\ Q_{bot,r} &= \int_{t_5}^{t} i_{ds,Q2}dt \\ &= Q_{oss}(v_{ds,Q2}(t)) - Q_{oss}(v_{dc}) \end{aligned} \tag{20}$$

In valley switching case, the current at t_6 is zero [32]. The remained energy at t_6 is dissipated in the GaN HEMT 2DEG [33].

In ZVS case, according to energy conservation,

$$\begin{aligned} &\frac{1}{2}Li_L^2(t_5) + (Q_{top,r} + Q_{bot,r})v_{ac} + E_{oss,Q1}(t_5) + E_{oss,Q2}(t_5) \\ &= \frac{1}{2}Li_L^2(t) + v_{dc}Q_{top,r} + E_{oss,Q1}(t) + E_{oss,Q2}(t) \end{aligned} \tag{21}$$

At t_5, $v_{ds,Q2} = v_{dc}$. At t_6, $v_{ds,Q2} = 0$. According to Fig. 6 (c), $E_{oss,Q1}(t_5) + E_{oss,Q2}(t_5) = E_{oss,Q1}(t_6) + E_{oss,Q2}(t_6)$. Hence, equation (21) can be rewritten as (22).

$$\begin{aligned} &\frac{1}{2}Li_L^2(t_5) + (Q_{top,r}(t_6) + Q_{bot,r}(t_6))v_{ac} \\ &= \frac{1}{2}Li_L^2(t_6) + v_{dc}Q_{top,r}(t_6) \end{aligned} \tag{22}$$

Considering both ZVS and valley-switching cases, at t_6, i_L is derived as (23).

B. Current Zero-Crossing Prediction

The on-time (T_{on}) counts from i_L zero-crossing point t_0 and ends at t_1. $T_{on} = t_1 - t_0$. The estimated inductor current ($i_{L,est}$) at the end of T_{on} is,

$$i_{L,est}(t_1) = \frac{v_{ac}}{L}T_{on} \tag{24}$$

The criteria for entering the nonpower transfer scenario relies on $i_L(t_1)$. i_L variation is estimated following the principle of energy conservation in the interval $t_1 \sim t_2$. If Q_1 can achieve ZVS turning-on, the circuit works in normal power transfer scenario.

The following equation holds.

$$\frac{1}{2}Li_L^2(t_1) + 2Q_{tot}v_{ac} = \frac{1}{2}Li_L^2(t_2) + v_{dc}Q_{tot} \tag{25}$$

where, Q_{tot} is the overall charge flowing through a single switch (Q_1 or Q_2) when its drain-source voltage rises from 0 to v_{dc}, $Q_{tot} \equiv Q_{oss}(v_{dc})$.

If $v_{ac} > (v_{dc} - v_{ac})$, (25) holds and $i_{L1}(t_2) > i_{L1}(t_1)$. $i_L(t_2)$ is always sufficient to enable the ZVS turning-on of Q_1. However, when $i_L^2(t_1) < -2K_1$, $K_1 = Q_{tot}(2v_{ac} - v_{dc})/L$, (25) does not hold and D_{Q1} never conducts. The circuit works in nonpower transfer scenario.

Hence, $i_{L,est}$ at t_2 is derived as follows,

$$i_{L,est}(t_2) = \begin{cases} \sqrt{i_{L,est}^2(t_1) + 2K_1}, & T_{on}^2 > -2K_1L^2/v_{ac}^2 \\ 0, & T_{on}^2 \le -2K_1L^2/v_{ac}^2 \end{cases} \tag{26}$$

$$i_L(t_6) = \begin{cases} \sqrt{i_L(t_5)^2 + \frac{2}{L}[Q_{top,r}(t_6)(v_{ac}-v_{dc}) + Q_{bot,r}(t_6)v_{ac}]}, & \text{ZVS case} \\ 0, & \text{Valley}-\text{switching case} \end{cases} \tag{23}$$

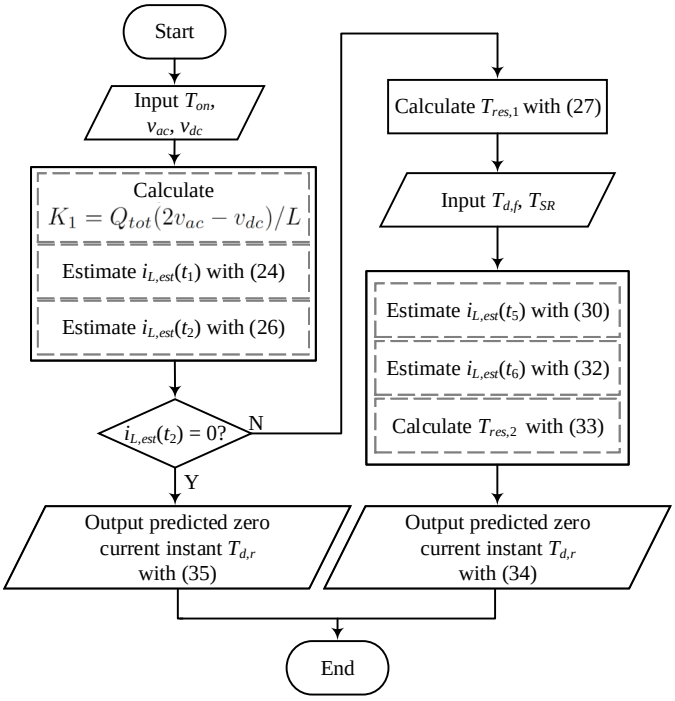


Fig. 7. Flowchart of the proposed current zero-crossing prediction algorithm.

$i_{L,est}(t_2)$ are different in normal power transfer scenario and nonpower transfer scenario, the current estimator runs in different cases.

1) normal power transfer scenario: The charge flow in the resonance $t_1 \sim t_2$ is very fast in the normal power transfer scenario. The resonant duration $T_{res,1} = t_2 - t_1$ is estimated by a trapezoid approximation as shown in Fig. 3 (a).

$$T_{res,1} = \frac{4Q_{tot}}{i_{L,est}(t_2) + i_{L,est}(t_1)} \tag{27}$$

The error between the actual deadtime $T_{res,1,act}$ and the approximated value $T_{res,1}$ at both light load and full load conditions are evaluated in Fig. 8. $T_{res,1,act}$ is achieved from simulation results considering the nonlinear $C_{oss} - v_{ds}$ properties.

As shown in Fig. 8 (a), the error decreases with the increase of power. At light load (150W), the estimated $T_{res,1}$ has a difference within $40ns$ compared with the actual $T_{res,1,act}$. The estimation error decreases with the increase of inductor current. From Fig. 8 (b), due to the minimum DSP EPWM step in the deadband, the difference between $T_{res,1,act}$ and $T_{res,1}$ at full load condition is within $5ns$. When the average inductor current rises, the error decreases. Therefore, the accuracy of the Trapezoid approximation in (27) is acceptable.

The inductor current in $t_2 \sim t_5$ is decreasing. $T_{d,f}$ is the deadband set by the controller after the active switch turns off.

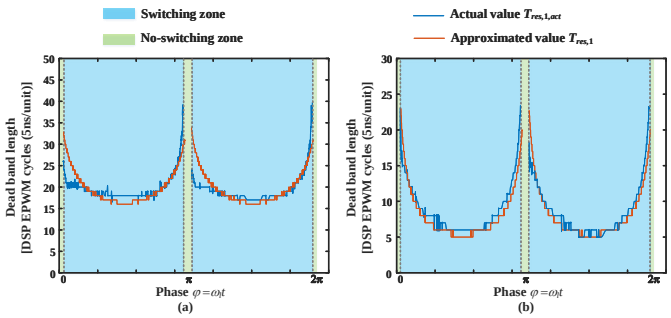


Fig. 8. Comparison between the actual deadtime $T_{res,1,act}$ and the approximated deadtime $T_{res,1}$ at (a) light load (150W) and (b) full load.

$T_{d,f}$ should be longer than $T_{res,1}$.

$$T_{d,f} = (t_3 - t_1) \geq T_{res,1} \tag{28}$$

T_{SR} is the SR switch conducting time, $T_{SR} = (t_5 - t_3)$. $i_{L,est}(t_5)$ is calculated as follows.

$$\begin{aligned} i_{L,est}(t_5) =& i_{L,est}(t_2) + \frac{v_{ac} - v_{dc}}{L} T_{SR} \\ &+ \frac{v_{ac} - v_{dc} - V_D}{L}(T_{d,f} - T_{res,1}) \end{aligned} \tag{29}$$

Since $v_{dc} - v_{ac} \gg V_D$, (29) can also be approximated as follows.

$$i_{L,est}(t_5) = i_{L,est}(t_2) + \frac{v_{ac} - v_{dc}}{L}(T_{SR} + T_{d,f} - T_{res,1}) \tag{30}$$

During $t_5 \sim t_6$, L resonates with the nonlinear C_{oss}. With energy conservation, the following equation yields.

$$\frac{1}{2}Li_L^2(t_5) + v_{dc}Q_{tot} = \frac{1}{2}Li_L^2(t_6) + 2Q_{tot}v_{ac} \tag{31}$$

When $v_{ac} < 0.5v_{dc}$, ZVS of Q_2 can be realized with a negative $i_L(t_6)$. Otherwise, the ZVS condition is determined by $i_L(t_5)$. If (31) doesn't hold, valley-switching is achieved, and ZVS is lost. $i_{L,est}$ at t_6 is derived as,

$$i_{L,est}(t_6) = \begin{cases} -\sqrt{i_{L,est}^2(t_5) - 2K_1}, & i_{L,est}^2(t_5) - 2K_1 > 0 \\ 0, & i_{L,est}^2(t_5) - 2K_1 \leq 0 \end{cases} \tag{32}$$

Since the inductor current starts or ends near zero, trapezoid approximation is not accurate to estimate the deadband before the turning on of Q_2. The resonance $T_{res,2} = t_6 - t_5$ in this zone is calculated via (7), (8).

$$T_{res,2} = \frac{\pi + \arctan\frac{i_{L,est}(t_5)Z_n}{v_{dc}-v_{ac}} + \arctan\frac{i_{L,est}(t_6)Z_n}{v_{ac}}}{\omega_n} \tag{33}$$

During $t_6 \sim t_7$, a freewheeling current flows through the equivalent body diode of Q_2. i_L follows (9). The deadband before the switch turning on is $T_{d,r}$. The zero-current prediction is achieved by controlling $T_{d,r}$.

$$T_{d,r} = t_7 - t_5 = -i_{L,est}(t_6)\frac{L}{v_{ac}+V_D} + T_{res,2} \tag{34}$$

2) nonpower transfer scenario: In the nonpower transfer scenario, the inductor resonates with C_{oss} of Q_1 and Q_2 during $t_1 \sim t_3$. $v_{ds,Q2}$ is the same at t_1 and t_3. Therefore, $i_L(t_3) = -i_L(t_1)$. Time parameters $T_{d,f}, T_{SR}, T_{d,r}$ are derived as,

$$\begin{aligned} T_{d,f} = t_3 - t_1 &= \frac{\pi + 2\arctan\frac{L}{Z_n T_{on}}}{\omega_n}, \\ T_{SR} = 0,\ T_{d,r} = t_4 - t_3 &= \frac{v_{ac}}{v_{ac}+V_D} T_{on} \end{aligned} \tag{35}$$

The entire process of the current zero-crossing prediction is illustrated in Fig. 7. With given T_{on}, v_{ac}, and v_{dc}, $i_{L,est}(t_1)$ and $i_{L,est}(t_2)$ are estimated. Then, if $i_{L,est}(t_2) > 0$, the normal power transfer model is used to predict the zero-current instant. Otherwise, the non-power transfer model is utilized.

C. Averaged Inductor Current Estimation

According to Fig. 4, the averaged inductor current $i_{L,avg}$ in non-power transfer zone is 0.

In normal power transfer scenario, i_L has two resonance intervals. Therefore, it is difficult to accurately estimate the averaged current in real-time based on simple calculations. On the other hand, the transient process is trivial compared with T_{on} or T_{SR}, the triangular approximation can be used to estimate the averaged inductor current. The peak current is approximated as $i_L(t_1)$. The valley current is derived via (8).

Taking both normal power transfer and nonpower transfer scenarios into consideration, the estimated averaged inductor current $i_{L,avg,est}$ is derived as,

$$i_{L,avg,est} = \begin{cases} 0, & T_{on}^2 \le -2K_1L^2/v_{ac}^2 \\ \dfrac{v_{ac}T_{on}Z_n - L(v_{dc}-v_{ac})}{2Z_nL}, & T_{on}^2 > -2K_1L^2/v_{ac}^2 \end{cases} \tag{36}$$

The error between the averaged inductor current $i_{L,avg,act}$ and the triangular approximated current $i_{L,avg,est}$ has been evaluated at light load and full load in Fig. 9. $i_{L,avg,act}$ is achieved from simulation results considering the nonlinearity of $C_{oss} - v_{ds}$.

The current waveform comparison of $i_{L,avg,act}$ and $i_{L,avg,est}$ at light load is shown in Fig. 9 (a). The triangular approximation is higher than the accurate value by 0.1A at the peak current point. In Fig. 9 (b), the triangular approximation is higher than the accurate value by 0.04A at the peak current point. This error is relatively minor. Meanwhile, the approximation effectively relieves the computation burden. Indeed, calculating the averaged inductor current in real-time is very complicated and time-consuming. In the proposed method, triangular approximation achieves a good compromise between model accuracy and real-time execution.

The iTHD of $i_{L,avg,act}$, and $i_{L,avg,est}$ at light load (150W) are 7.47% and 1.97%, respectively. The iTHD of $i_{L,avg,act}$ and $i_{L,avg,est}$ at full load are 4.17% and 1.65%, respectively.

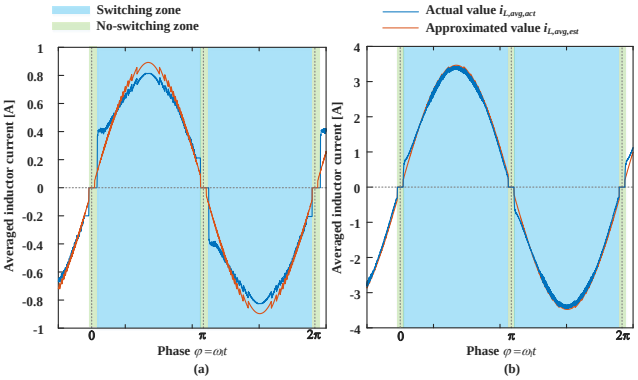


Fig. 9. Comparison between the averaged inductor current $i_{L,avg,act}$ and the triangular approximated current $i_{L,avg,est}$ at (a) light load (150W) and (b) full load.

The $S_3 - S_4$ commutation deadband (green zone) degrades the iTHD of $i_{L,avg,est}$. The approximation accuracy in the proposed method increases with the increase of power.

IV. Current Estimator-based CRM PFC control

A. Disturbance Damping

In PFC applications, disturbance from the inductance variation and parasitic resistance may inject distortion to the estimator, which brings error to the current zero-crossing prediction.

In Fig. 10, the inductor current waveforms in ideal and disturbed cases are plotted. Fig. 8 (a) demonstrates the natural ZVS case and Fig. 8 (b) illustrates the valley-switching case. Fig. 8 (c) shows the ZVS extension case. The green dashed curve corresponds to the ideal case.

Ideally, SR should be turned off at $i_{val1,ideal}$.

$$i_{val1,ideal} = \begin{cases} 0, & v_{ac} \le 0.5v_{dc} \\ 0, & v_{ac} > 0.5v_{dc} \text{ with valley switching} \\ \sqrt{2K_1}, & v_{ac} > 0.5v_{dc} \text{ with ZVS Extension} \end{cases} \tag{37}$$

Adding a disturbance Δi on the turning-off current gives the blue curve $i_{val1}(n)$.

$$i_{val1}(n) = i_{val1,ideal} + \Delta i \tag{38}$$

In Fig. 10, the disturbance provides additional backflow current for ZVS of Q_2. During the resonance, the actual inductor current changes to $i_{val2}(n)$.

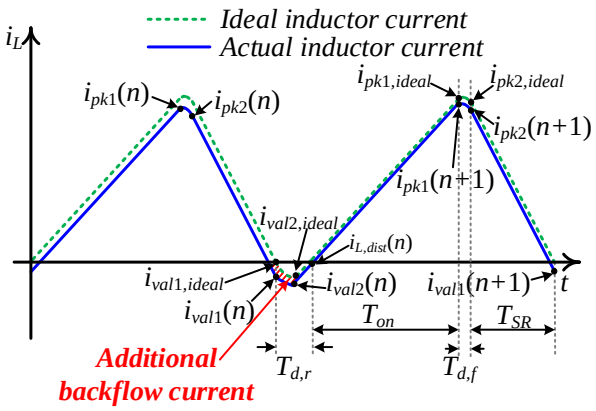
$$i_{val2}(n) \approx \begin{cases} -\sqrt{-2K_1 + i_{val1}^2(n)}, & K_1 < i_{val1}^2(n)/2 \\ 0, & K_1 \ge i_{val1}^2(n)/2 \end{cases} \tag{39}$$

Compared with the ideal current $i_{val2,ideal}$,

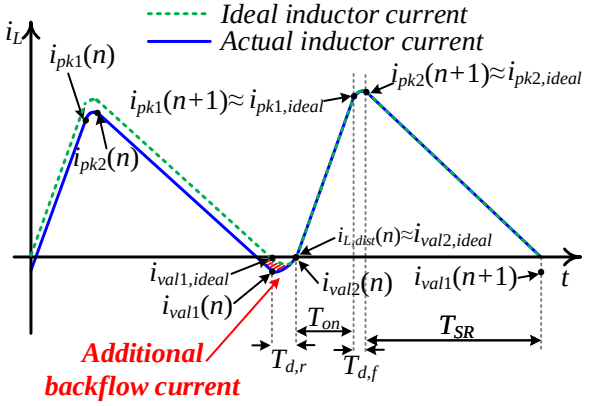
$$i_{val2,ideal} = \begin{cases} -\sqrt{-2K_1}, & v_{ac} < 0.5v_{dc} \\ 0, & v_{ac} \ge 0.5v_{dc} \end{cases} \tag{40}$$

The ideal peak current is approximated as twice the input averaged current. $V_{ac,RMS}$ is the root-mean-square (RMS) of v_{ac}.

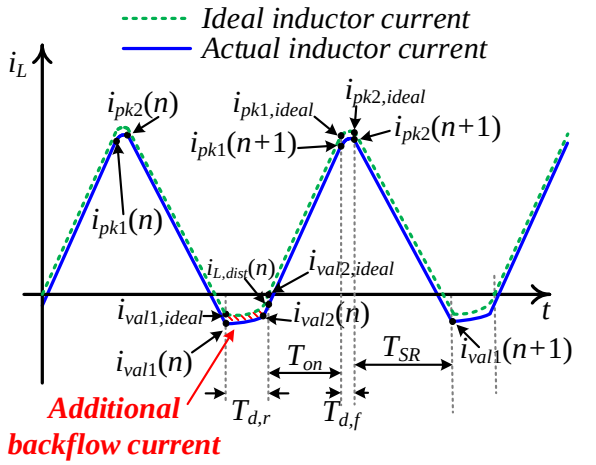
$$i_{pk1,ideal} \approx \frac{2v_{ac}P_{dc}}{V_{ac,RMS}^2} \tag{41}$$



(a)



(b)



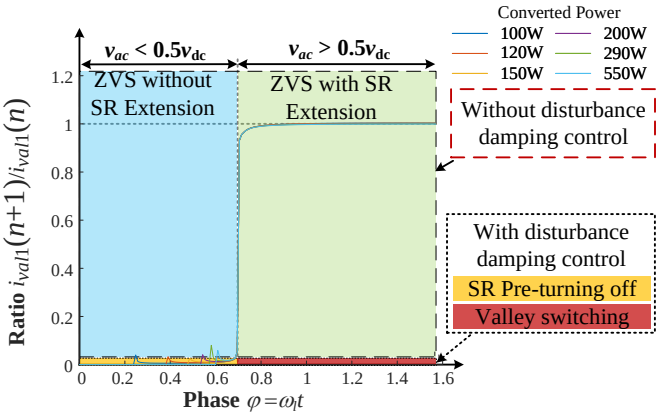
(c)

Fig. 10. Waveform with additional SR conduction time by minimum time-length of DSP (a) ZVS case, (b) valley-switching case, (c) ZVS extension case.

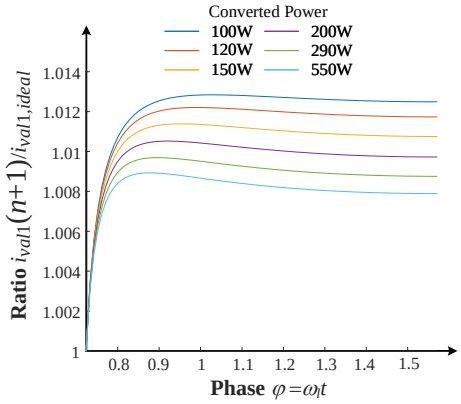
The disturbed current $i_{val2}(n)$ charges C_{oss} faster than $i_{val2,ideal}$. The time difference is,

$$\Delta t(n) = \frac{1}{\omega_r}\left(\arctan\frac{Z_n i_{val2,ideal}}{v_{ac}} - \arctan\frac{Z_n i_{val2}(n)}{v_{ac}} + \arctan\frac{Z_n i_{val1}(n)}{v_{ac}-v_{dc}} - \arctan\frac{Z_n i_{val1,ideal}}{v_{ac}-v_{dc}}\right) \tag{42}$$

At the end of $T_{d,r}$, the disturbed current $i_{L,dist}$ may cross



(a)



(b)

Fig. 11. Ratio of (a) $i_{val1}(n+1)/i_{val1}(n)$ (b) ZVS Extension case $i_{val1}(n+1)/i_{val1,ideal}$ under different loads.

zero. Since the GaN 2DEG is not conducted, the disturbed inductor current cannot be positive.

$$i_{L,dist} = \begin{cases} i_{val2}(n) + \Delta t(n)\dfrac{v_{ac}}{L}, & \Delta t(n) < -\dfrac{i_{val2}(n)L}{v_{ac}} \\ 0, & \Delta t(n) \geq -\dfrac{i_{val2}(n)L}{v_{ac}} \end{cases} \tag{43}$$

The actual current $i_{pk1}(n+1)$ is yielded as,

$$i_{pk1}(n+1) = -i_{val2,ideal} + i_{L,dist}(n) + i_{pk1,ideal} \tag{44}$$

$i_{pk2}(n+1)$ is

$$i_{pk2}(n+1) = \sqrt{2K_1 + i_{pk1}^2(n+1)} \tag{45}$$

Ideally, $i_{pk2,ideal}$ is,

$$i_{pk2,ideal} = \sqrt{2K_1 + i_{pk1,ideal}^2} \tag{46}$$

The SR turning-off current by iterative error at the next switching cycle is,

$$i_{val1(n+1)} = i_{pk2}(n+1) - i_{pk2,ideal} + i_{val1,ideal} \tag{47}$$

In Fig. 11 (a), the ratio of $i_{val1}(n+1)/i_{val1}(n)$ is plotted. The blue zone is the natural ZVS case without SR extended conduction. The green zone is the ZVS with SR extension. The yellow zone is ZVS with SR pre-turning off. The red

zone is the valley switching case. Except for the green zone, the ratio is below unity, which means that the disturbance will be damped. In the green zone, the ratio increases to unity as the v_{ac} increases. This indicates that the disturbance damping performance at the ZVS extension case degrades as the v_{ac} increases. To better illustrate it, in Fig. 11 (b), the ratio of $i_{val1}(n+1)/i_{val1,ideal}$ in ZVS extension case is plotted. The ratio is greater than unity, which means that the disturbance will be accumulated at the next switching cycles and make $i_{L,est}$ lose tracking of i_L. On the other hand, in the valley switching case, the disturbance damped to zero at the next switching cycle. For conventional ZCD-circuit-based design, ZVS extension can achieve full load range ZVS, and the disturbance will be eliminated with the ZCD signal. In contrast, for the proposed current estimator-based control, no ZCD signal is available. For the ZVS extension case, it needs a disturbance observer [34] to eliminate the disturbance effect, which complicates the design. Valley switching simplifies the control algorithm with dead-beat disturbance-damping performance.

The proposed disturbance damping control consists of SR pre-turning off and valley switching. It alternates the SR conduction time. By pre-turning off the SR switch at $i_{L,est}$ zero-crossing point, no additional negative current will be injected into the inductor current. SR is pre-turned off before $i_{L,est}$ zero-crossing when $v_{ac} \leq 0.5$vdc. When $v_{ac} > 0.5v_{dc}$, valley switching is realized. Therefore, $i_{val,1}$ is always zero in the whole line period.

To realize the proposed disturbance damping control, k_{po} is defined as the conduction ratio of the SR MOSFET turning-on time. T_{SR} is,

$$T_{SR} = \left(\frac{i_{L,est}(t_2)L}{v_{dc} - v_{ac}} - T_{d,f} + T_{res,1} \right) k_{po} \tag{48}$$

The SR on-time is alternated. To keep the switching frequency unchanged, $T_{d,r}$ should be extended,

$$T_{d,r} = \begin{cases} T_{res,2} + \dfrac{L\sqrt{-2K_1}}{v_{ac}+V_D} \\ \quad +T_{SR}\dfrac{1-k_{po}}{k_{po}}, & K_1 \leq 0 \ \& \ i_{L,est}(t_2) > 0 \\ \dfrac{v_{ac}}{v_{ac}+V_D}T_{on}, & K_1 \leq 0 \ \& \ i_{L,est}(t_2) = 0 \\ \dfrac{\pi}{\omega_n} + T_{SR}\dfrac{1-k_{po}}{k_{po}}, & K_1 > 0 \end{cases} \tag{49}$$

In summary, with the proposed disturbance damping control, if a certain negative current is induced by disturbance, pre-turning off SR near the inductor current zero-crossing point can suppress the estimator error. Since the inductor current is near zero, the increased conduction loss is trivial.

B. System Implementation

The block diagram of the proposed controller is illustrated in Fig. 12. To attenuate the injection of differential-mode i_L into the grid, an LC filter that consists of C_{ac} and L_{DM} is added. There are two interrupt service routines (ISR_1, ISR_2) running at $10Hz$ and $40\text{k}Hz$, respectively. Gating signals for

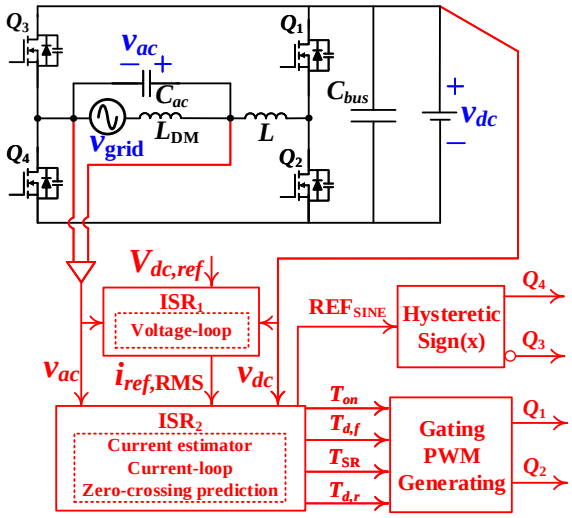


Fig. 12. Block diagram of the proposed controller.

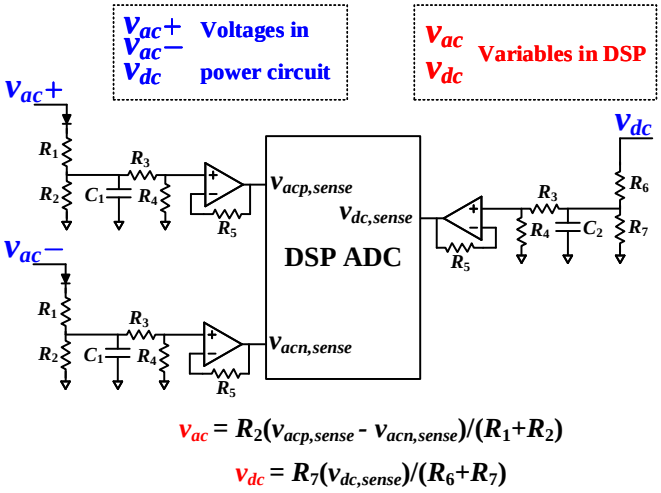


Fig. 13. Schematic of peripheral circuits to sample v_{ac} and v_{dc}.

Q_1 and Q_2 are generated with given time parameters T_{on}, $T_{d,f}$, T_{SR}, and $T_{d,r}$.

The signals to be sampled and connected to the peripheral of the DSP in the proposed methodology includes input voltage v_{ac} and output voltage v_{dc}. In Fig. 12, v_{ac} and v_{dc} are sampled and fed into the controller with the generated PWM parameters, including on-time, deadband, and SR time. The current estimator rebuilds the inductor current at the switching transition instants. Moreover, the inductor's current zero-crossing point can be predicted with the current estimator. Therefore, no inductor current sampling is required. It is also the highlight of the proposed method.

To send the two voltage signals of the power circuit to the DSP, a signal acquisition circuit is designed as shown in Fig. 13. First, the voltage on the power circuit would pass through a voltage divider with a low pass filter. The low pass filter is used to filter the sensing noise. Then, a voltage follower buffers the voltage signal and sends it to the DSP ADC.

Function blocks of ISRs are presented in Fig. 14.

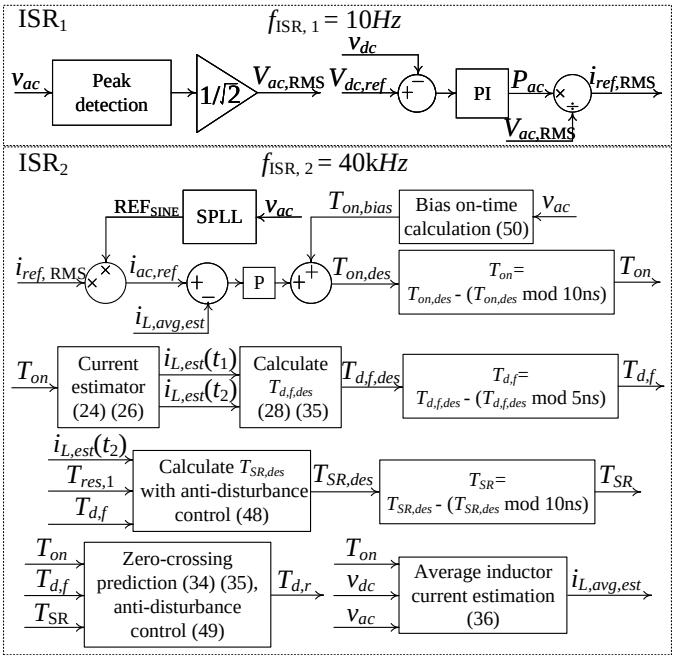


Fig. 14. Function details in ISR_1 and ISR_2.

ISR_1 is in charge of low bandwidth algorithms, such as the calculation of the RMS of ac side voltage and PFC voltage-loop compensation. v_{ac}'s peak voltage is detected. Then, the RMS voltage of the ac side $v_{ac,\mathrm{RMS}}$ is obtained. The error between output voltage $V_{dc,ref}$ and the feedback dc-link voltage v_{dc} is fed to the voltage loop of the PI compensator. The compensator gives the desired input power P_{ac}. Dividing P_{ac} by $v_{ac,\mathrm{RMS}}$, the demanded RMS current of ac side $i_{ref,\mathrm{RMS}}$ can be obtained.

ISR_2 is in charge of algorithms such as software phase-lock-loop (SPLL) [35], estimator-based inner current loop, current zero-crossing prediction, and the averaged current estimator. SPLL generates a uniform sinusoidal signal $\mathrm{REF}_{\mathrm{sine}}$ that is in phase with v_{ac}. The product of $\mathrm{REF}_{\mathrm{sine}}$ and $i_{ref,\mathrm{RMS}}$ provides the reference instantaneous input current $i_{ac,ref}$. In the inner current loop, the conventional current sensor is replaced with the proposed current estimator. Error between $i_{ac,ref}$ and $i_{L,est}$ is fed to a proportional unit. By adding a bias on-time $T_{on,bias}$, the desired on-time $T_{on,des}$ is determined. $T_{on,des}$ leads the average inductor current to follow the desired waveform $i_{ac,ref}$. $T_{on,bias}$ is the bias on-time. The proportional controller is the trade-off between the control accuracy and the response speed of $T_{on,des}$. $i_{L,est}$ is not equal to $i_{ac,ref}$ all the line cycle. There's a round-off error due to the discrete characteristic of DSP. For example, $T_{on,bias}$ may be calculated as $733ns$. However, the DSP can only generate a PWM waveform with on-time $730ns$. This means the actual T_{on} has a minor deviation (within $10ns$) compared with the biased on-time $T_{on,bias}$. It results that $i_{L,est}$ would be a bit different from $i_{ac,ref}$. Adding a compensator can mitigate the difference. A PI compensator has good accuracy. However, it may incur oscillation with improper parameters and increase the THD. Since the difference is trivial, the proportional controller with fast response and no oscillation can be used.

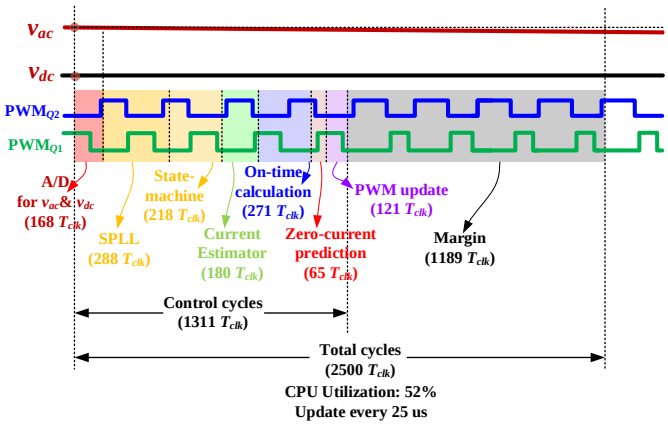


Fig. 15. DSP clock cycles of code computation and execution with the proposed zero-current predicting algorithm.

Since nonpower transfer scenario doesn't deliver real power, $T_{on,bias}$ is derived from the normal power transfer scenario.

$$T_{on,bias} = \frac{2Z_n L i_{ac,ref} + L(v_{dc} - v_{ac})}{v_{ac} Z_n} \tag{50}$$

$T_{on,des}$ is a float number, and it may not be integer times of PWM resolution time ($10\mathrm{n}s$ for PWM counter and $5\mathrm{n}s$ for deadband blocks). Considering the discretizing process of a digital system, the executed on-time T_{on} is estimated. Using the executed on-time in the current estimator reduces the error induced by discretizing in digital control. The process is similar for the desired deadband $T_{d,f,des}$ and desired SR on-time $T_{SR,des}$.

$$\begin{aligned} T_{on} &= T_{on,des} - (T_{on,des} \bmod 10\mathrm{n}s) \\ T_{d,f} &= T_{d,f,des} - (T_{d,f,des} \bmod 5\mathrm{n}s) \\ T_{SR} &= T_{SR,des} - (T_{SR,des} \bmod 10\mathrm{n}s) \end{aligned} \tag{51}$$

Also, the process in (51) is to achieve a more accurate $T_{d,r}$ and $T_{d,r}$ doesn't need to do that estimation. Finally, the averaged inductor current under the given T_{on}, v_{dc}, and v_{ac} are estimated. It will be fed into the current loop in the next execution of ISR_2.

Fig. 15 gives the DSP clock cycles of code computation and execution. At the beginning of an iteration, sampling and filtering of v_{ac} and v_{dc} take about 168 clock cycles (T_{clk}). Then, it takes 288 T_{clk} for SPLL to generate the reference sinusoidal signal ($\mathrm{REF}_{\mathrm{SINE}}$). With $\mathrm{REF}_{\mathrm{SINE}}$, the state machine determines whether to turn on Q_3, Q_4 in 218 T_{clk}. Next, the current estimator is executed with the previous on/off time in 180 T_{clk}. On-time calculation is alternated with the estimated averaged inductor current in 271 T_{clk}. Zero-crossing prediction is executed in 65 T_{clk}. Consequently, PWM parameters are updated in another 121 T_{clk}. The entire control process takes 1311 T_{clk}. Meanwhile, certain redundancy should be reserved for other tasks. In our design, 1189 T_{clk} is reserved for each iteration, which corresponds to 52% CPU utilization.

In Fig. 16, the relationship between inductor current zero-crossing and the zero-current prediction between two different switching cycles is illustrated. The ISR_2 predicts the inductor current zero-crossing point every $25\mu s$ as shown in Fig. 15.

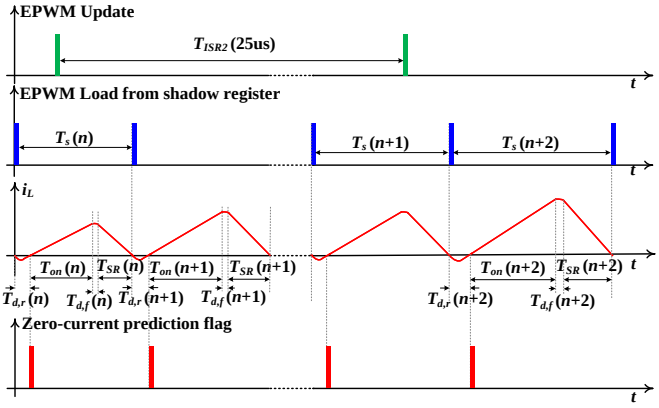


Fig. 16. Inductor current zero-crossing versus zero-current prediction between two different switching cycles.

TABLE II
DESIGN PARAMETERS

Parameters	Value
L	30 μH
Q_1, Q_2	LMG3410R070
Q_3, Q_4	IPW60R180P7
Rated output voltage v_{dc}	$400V$
Rated ac input v_{ac}	$220V_{\rm rms}$
Rated power	$550W$
C_{bus}	$1.2{\rm m}F$
Switching frequency range	$150{\rm k}Hz$-$1.6{\rm M}Hz$

When the prediction is updated, the flag EPWM Update is triggered. The shadow register of EPWM module is updated with $T_{on}(n+1)$, $T_{d,r}(n+1)$, $T_{SR}(n+1)$, $T_{d,f}(n+1)$. At the next PWM switching cycle, the data in the shadow register is loaded into the active register. The zero-current is predicted on the turning-on instant of Q_2 for positive half line cycle and Q_1 for negative half line cycle.

V. EXPERIMENTAL RESULTS

As a proof of concept, a $550W$ rated $220V$ to $400V$, totem pole Boost PFC converter prototype is designed. The key design parameters are summarized in Table II. The photograph

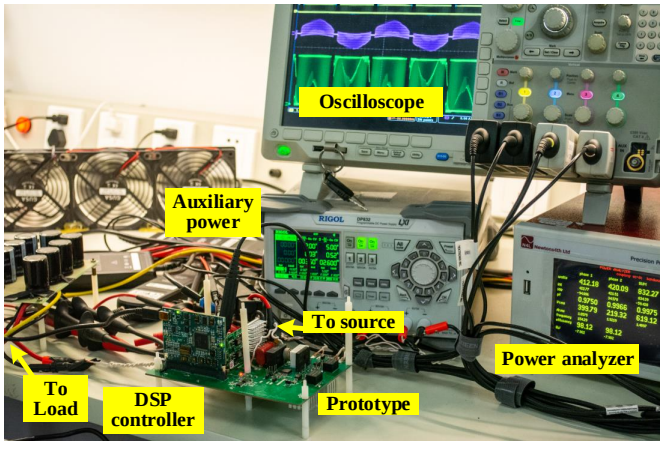
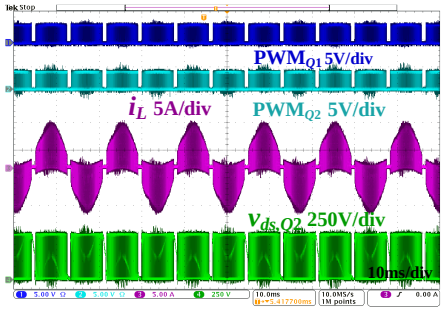
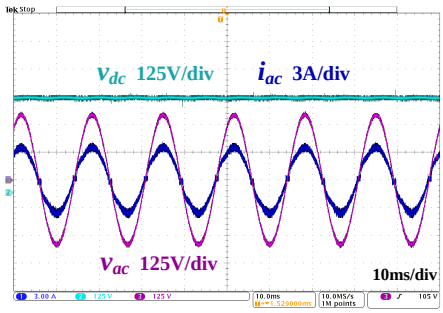


Fig. 17. Picture of the laboratory test bench.



(a)



(b)

Fig. 18. Key waveforms under 220V line input and 400V dc output at full load: (a) driving signals of $Q_{1,2}$, i_L, and $v_{ds,Q2}$; (b) v_{ac}, v_{dc}, and i_{ac}.

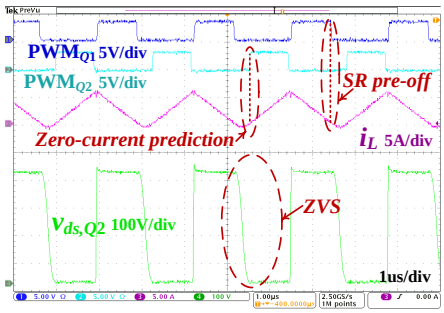


Fig. 19. ZVS waveforms when $v_{ac} < 0.5v_{dc}$ at full load.

of the test bench is given in Fig.17. TMS320F280049C from Texas Instruments is used to implement the digital control algorithms. GaN devices with integrated gate drivers are used for the high speed half-bridge. The peak switching frequency is $1.6{\rm M}Hz$. In the experimental setup, heat sinks aided by air cooling are used for cooling.

At full load, the steady-state experimental waveforms are captured in Fig. 18. Since $Q_{1,2}$ are GaN devices with integrated gate-drivers, no direct v_{gs} can be measured [36]. The time delay between v_{gs} and the driving signal is less than $20ns$. In the experiment, PWM signals are used to identify the gate driving signals, ${\rm PWM}_{Q1}$ for $v_{gs,Q1}$ and ${\rm PWM}_{Q2}$ for $v_{gs,Q2}$. i_L is at the boundary of DCM/CCM with a small negative current. $v_{ds,Q2}$ is measured. The envelope of $v_{ds,Q2}$ is clear. Input ac current i_{ac} is in phase with the input ac voltage. Voltage of dc-link v_{dc} is monitored.

A zoom-in of Fig. 18 at positive v_{ac} is captured in Figs. 19, 20. Fig. 19 demonstrates the ZVS when $v_{ac} < 0.5v_{dc}$. Fig. 20 captures the valley-switching when $v_{ac} > 0.5v_{dc}$. Zero-current

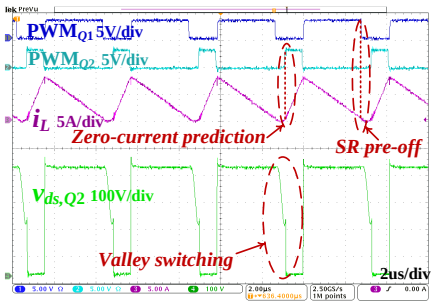
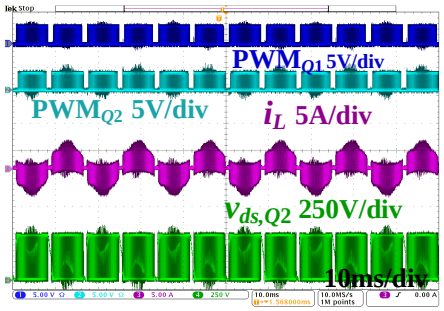
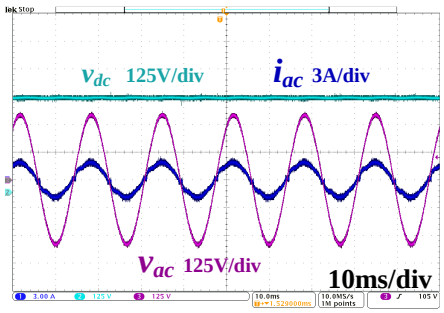


Fig. 20. Waveforms of valley-switching when $v_{ac} > 0.5v_{dc}$ at full load.



(a)



(b)

Fig. 21. Key waveforms under 220V line input and 400V dc output at half load: (a) driving signals of $Q_{1,2}$, i_L, and $v_{ds,Q2}$; (b) v_{ac}, v_{dc}, and i_{ac}.

prediction is validated in both scenarios. The gating signal of Q_1 falls before i_L crosses zero. This validates the effectiveness of the proposed disturbance-damping control.

In Fig. 21, the steady-state experimental waveforms are captured at half load. i_L is at the boundary of DCM/CCM with a small negative current. The envelope of $v_{ds,Q2}$ is clear. i_{ac} is in phase with the input ac voltage. The ripple voltage of v_{dc} is smaller than that in full load condition.

Figs. 22, 23 capture the zoom-in of Fig. 21 at positive v_{ac}. Fig. 22 monitored the ZVS when $v_{ac} < 0.5v_{dc}$. Fig. 23 demonstrates the valley-switching when $v_{ac} > 0.5v_{dc}$. In both scenarios, zero-current prediction is validated. With the proposed disturbance damping control, the gate signal of Q_1 falls before i_L crosses zero.

Near zero-crossing of v_{ac}, the desired average current is relatively small and v_{ac} changes rapidly. Moreover, the converter's boost ratio is very high, which brings a large duty cycle and a small switching period. In this situation, the influence of control delay on the estimated current becomes significant. This may lead to a loss of tracking of the estimator

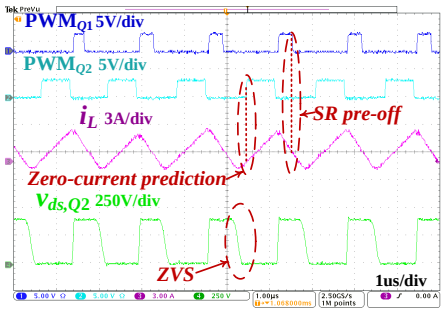


Fig. 22. ZVS waveforms when $v_{ac} < 0.5v_{dc}$ at half load.

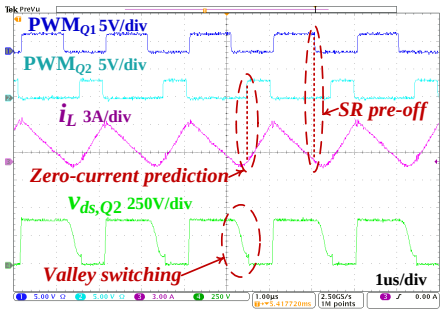


Fig. 23. Waveforms of valley-switching when $v_{ac} > 0.5v_{dc}$ at half load.

and additional THD. Therefore, both Q_1 and Q_2 remain off in a no-switching state and the inductor current stays zero when v_{ac} is near zero-crossing. Since the duration of the no-switching zone is short compared with the whole line cycle (less than 5%), and the desired averaged current in this zone is also small, the harmonic components introduced by the no-switching zone are high order, low amplitude. The impact on THD by the no-switching state is trivial.

The harmonic components of i_{ac} at 550W output power (full load) are plotted in Fig. 24. The harmonic components are lower than 3.6% of the fundamental component.

The input current THD (iTHD) is measured at different output power. The results are recorded in Fig. 25. The lowest iTHD is 5.4% at 427W output power.

The power factor correction performance under different load conditions is presented in Fig. 26. Correspondingly, Fig. 27 demonstrates the efficiency trend. As shown, the designed

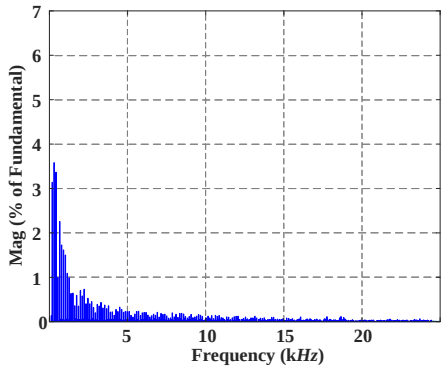


Fig. 24. FFT analysis with $v_{ac} = 220Vrms$, $v_{dc} = 400V$, full load (550W) condition.

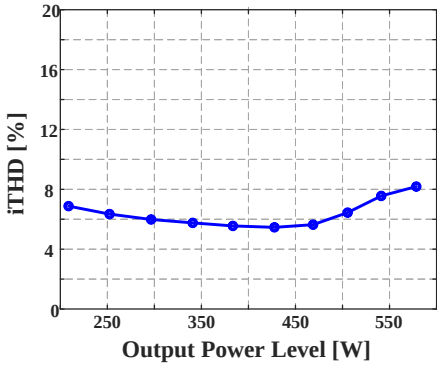


Fig. 25. Measured iTHD versus output power under 220Vac input.

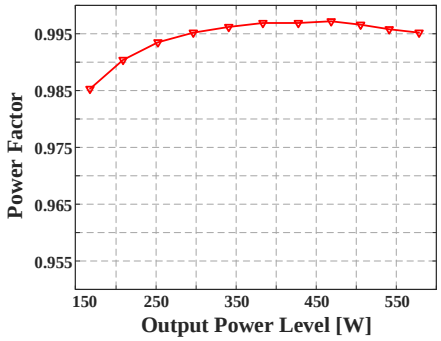


Fig. 26. Measured power factor versus output power.

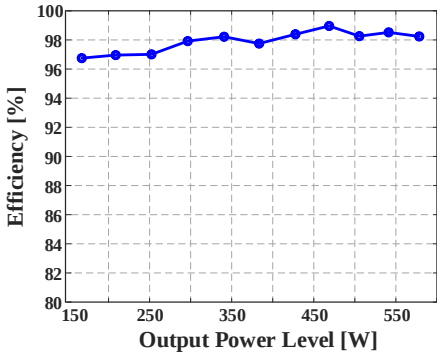


Fig. 27. Measured efficiency versus output power.

prototype exhibits 98.96% peak efficiency with 0.9972 power factor. As shown, high efficiency and high power factor are maintained over a wide load range.

VI. Conclusion

In this manuscript, a novel current sensorless CRM control is proposed for totem-pole Boost PFC converters. It utilizes an inductor current estimator model to estimate the averaged current and to predict the current zero-crossings. Compared with the conventional methods, the inductor current sensing signal and the zero-current detecting circuit are no longer required. The control loop and the peripheral circuit are simplified. The behavior of the estimator considering switching device C_{oss} model is analyzed and detailed. A disturbance damping control is proposed to mitigate the variation of inductance and parasitic resistance and improve the prediction accuracy. The operation principles, digital implementation, and estimation error suppression are discussed.

The proposed concept is verified in a $550W$-rated experimental prototype. With the proposed control scheme, the zero-crossing point of the inductor current is predicted. Valley-switching and zero-voltage switching are realized at the predicted zero-crossing points. The experiment results exhibit 98.96% peak efficiency with 0.9972 power factor. Good power factor and efficiency performances are achieved over a wide load range.

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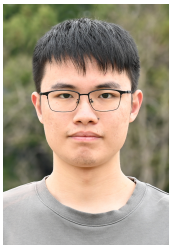

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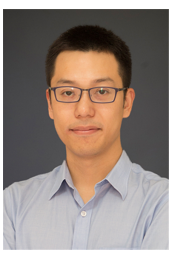

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