An H5-Bridge-Based Laddered $CLLC$ DCX With Variable DC Link for PEV Charging Applications

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***Abstract*—Plug-in electric vehicles' charger is preferred to cover an ultrawide battery voltage range with the vehicle-to-grid capability. Conventional bidirectional resonant dc–dc converters suffer from the contradiction among wide voltage gain range, squeezed dc-link voltage span, and narrow switching frequency band. To solve the issue, this article proposes a novel H5-bridge-based bidirectional $CLLC$ converter. By configuring the switch pattern, the H5-bridge can form the modes of single half-bridge, dual half-bridge, half full-bridge, and dual full-bridge, respectively. Correspondingly, six gain curves can be derived. Combined with the variable dc-link framework, the converter constrains the switching frequency in the vicinity of the resonant frequency with optimal efficiency. The converter achieves an ultrawide battery voltage range with a squeezed dc-link span. A bidirectionally synchronous rectification method is proposed to improve the efficiency further. To verify the proposed concept, a 1-kW rated prototype with a 320–420 V dc link is built and tested. It validates the battery voltage 55–420 V for charging and 230–420 V for discharging. Zero-voltage turn-ON and zero-current turn-OFF are achieved in the rectifying MOSFETs. The prototype exhibits 98.04% peak efficiency and good overall efficiency performance.**

***Index Terms*—Bidirectional, $CLLC$, dc transformer (DCX), H5-bridge, synchronous rectification (SR), wide voltage range.**

I. Introduction

A LI-ION battery is the dominant high-power battery in plug-in electric vehicles (PEV) [1], [2]. The terminal voltage of the Li-ion battery varies with the change of the battery state of charge. Correspondingly, the output of the PEV charger needs to be adapted to an ultrawide voltage range during the charging process [3], [4]. On the other hand, the vehicle-to-grid (V2G) technology requires the battery charger to deliver power bidirectionally [5]–[7].

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LLC resonant converters are promising in PEV charging applications due to their full-range zero-voltage switching (ZVS) [8], [9]. However, to achieve an ultrawide battery voltage range, a wide switching frequency (f_s) span is always required with frequency modulation (FM), which leads to performance degradation. Specifically, with f_s below resonance, the conduction loss increases rapidly. With f_s above resonance, the switching loss increases dramatically. The optimized parameter design can squeeze the f_s span with small magnetizing inductance (L_m). However, it leads to significantly increased conduction loss [10].

Many studies focus on extending the gain range of the LLC converter with constrained f_s span. In [11], with phase shedding in the multiphase resonant converter, the gain range can be extended. In [12], an H5-reconfigurable-bridge-based converter is proposed with four gain curves. In [13], an asymmetric H5-bridge-based LLC converter provides six gain cases. In [14], a hybrid converter merges a full-bridge converter and an LLC resonant converter to provide diverse gain properties. With those methods, the voltage gain range can be multiplied under a narrow f_s span. Consequently, the ultrawide battery voltage range can be fully covered with improved efficiency.

Although these methods can achieve an ultrawide charging voltage range, bidirectional power flow is not provided. To solve this deficiency, the authors of [15]–[23] put forward the bidirectional solutions. In [15], a pulsewidth modulation (PWM) control scheme is proposed. The duty cycle and the phase shift in the inverter legs are modulated to generate a three-level voltage for the resonant tank. Turn-OFF delay-control [16] and phase-shift [17] methods are utilized to broaden the voltage gain range. Despite that f_s is fixed at resonant frequency (f_r) in [15]–[17], conduction loss increases rapidly with the increase in the phase shift. In [18], by adding a notch filter on LLC, both fundamental and third harmonics deliver power. Therefore, the bidirectional voltage gain range can be extended. In [19], an auxiliary four-quadrant switch is added to the battery-side bridge. Half-bridge and full-bridge modes can be provided. By changing the duration of the half-bridge mode, a wide normalized gain range can be achieved. In [20] and [21], a bidirectional $CLLC$ converter with FM control is investigated. In [22], a flying-capacitor-based three-level bridge is proposed with four gain modes. In [23], an asymmetric parameter $CLLC$ resonant converter is proposed to adapt to a wide battery voltage range.

The aforementioned methods effectively extend the voltage gain range with a narrow f_s span for bidirectional power flow.

However, with the fixed dc-link framework, the main loss is still contributed by the dc–dc stage [24]. Low efficiency occurs at margin gain. To improve, a variable dc-link framework is investigated in [24]–[28]. The voltage gain requirement of the dc–dc stage is significantly alleviated. In [25] and [26], the ac–dc stage provides an expanded dc-link voltage span. Nevertheless, the span is not wide enough so that the dc–dc stage still works with low efficiency at margin gain. In [27] and [28], the dc–dc stage operates at f_s close to f_r to optimize the efficiency, whereas the major conversion ratio is yielded by the ac–dc stage. The variable dc-link framework can alleviate the conversion stress and resolves the tradeoff between the wide voltage gain range and the narrow f_s span. However, another issue arises. A wide dc-link voltage span is required to cover an ultrawide battery voltage range.

H5-bridge-based LLC converters are proposed in [12] and [13]. 97.05% and 97.64% peak efficiency can be achieved, respectively. However, those works mainly focus on unidirectional power flow. Moreover, synchronous rectification (SR) is not implemented. Indeed, SR in these topologies is complicated due to the uneven load distribution. Moreover, the body diode may conduct by the freewheeling current, causing additional conduction loss. The proposed work resolves those issues with 98.04% peak efficiency and overall higher efficiency.

On the other hand, the previous work shows that both reconfigurable resonant converters [11]–[14], [22] and the variable dc-link framework [24]–[28] can squeeze the switching frequency range. However, the interaction of those two methodologies is rarely researched. What is more, in the emerging V2G applications, the LLC converter may have dc bias current due to the mismatch of different loop parameters, which is challenged for bidirectional operation [29]. To fix this problem, empirical methods use a bulky capacitor serially connected on the secondary side or adopts a $CLLC$ resonant tank. In this work, to compensate the reactive power by the leakage inductance on the secondary side [30], the $CLLC$ resonant tank is utilized.

This article focuses on the bidirectional on-board charger with ultrawide battery voltage range. Compared with the investigated works, this work has: 1) new H5-bridge configuration scheme to reduce conduction loss; 2) new resonant tank with the H5-bridge topology and its corresponding gain estimation model without consideration for load distribution in resonant tanks; 3) investigation of the variable dc-link voltage framework cooperation with a reconfigurable converter in PEV charging applications; and 4) bidirectional operation of the H5-bridge converter with the proposed SR scheme. Based on these features, higher efficiency and simpler control method can be achieved for an ultrawide-range bidirectional battery charger. This is the main contribution of the proposed work.

The rest of this article is organized as follows. Section II introduces the proposed bidirectional reconfigurable H5-bridge converter. Section III analyzes the gain properties. The SR method is presented in Section IV. Features of the laddered dc transformer (DCX) with the variable dc-link framework are described in Section V. Experimental verification is demonstrated in Section VI. Finally, Section VII concludes this article.

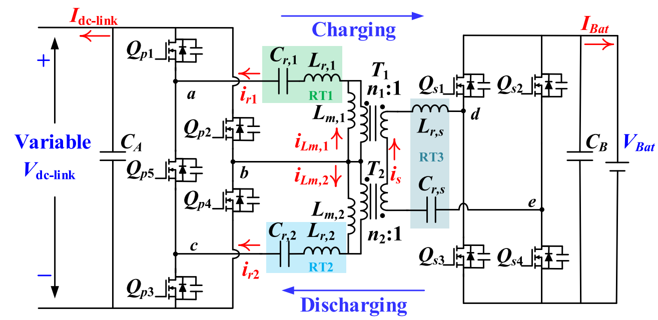


Fig. 1. Schematic of the proposed bidirectional H5-bridge-based $CLLC$ DCX.

II. Proposed H5-Bridge-Based Laddered $CLLC$ DCX

Fig. 1 shows the schematic of the proposed converter. The output ports of the H5-bridge (v_{ab} and v_{bc}) serve as the inputs of two resonant tanks, RT1 and RT2, respectively. RT1 consists of $C_{r,1}$ and $L_{r,1}$. RT2 consists of $C_{r,2}$ and $L_{r,2}$. A full active bridge is adopted on the battery side. A series-connected capacitor $C_{r,s}$ is installed to compensate the lumped leakage inductance $L_{r,s}$ of dual transformers T_1 and T_2 to reduce the reactive power. $L_{m,1}$ and $L_{m,2}$ are magnetizing inductances of T_1 and T_2, respectively. T_1 has turns ratio n_1. T_2 has turns ratio n_2. It should be noted that the resonant frequencies of RT1, RT2, and RT3 are matched, which means $C_{r,1}L_{r,1} = C_{r,2}L_{r,2} = C_{r,s}L_{r,s} = 1/(2\pi f_r)^2$.

A. Bidirectional Reconfiguration Strategy

The resonant currents i_{r1}, i_{r2}, and i_s, port voltages v_{ab} and v_{bc} and the H5-bridge gate signals $v_{gs,p1\sim5}$ in the proposed bidirectional converter are shown in Fig. 2 for the charging process and in Fig. 3 for the discharging process.

For PEV, the required charging voltage range is broader than that in the discharging process. Therefore, six reconfigurable charging modes and three reconfigurable discharging modes are utilized. Notation of mode: "-C" means charging and "-D" means discharging.

$\mathrm{PWM_A}$ and $\mathrm{PWM_B}$ are FM signals. In the charging process, $\mathrm{PWM_A}$ and $\mathrm{PWM_B}$ lead the full-bridge gating signals. The net power delivered by v_{ab} and v_{bc} is positive. Power is transferred from the dc link into the battery side. In the discharging process, $\mathrm{PWM_A}$ and $\mathrm{PWM_B}$ lag the full-bridge gating signals. The net power delivered by v_{ab} and v_{bc} is negative. Power is transferred from the battery to the dc link. Without loss of generality, n_2 is smaller than n_1 for analysis. The description of the reconfigurable modes is as follows.

1) Mode 1-C: Q_{p2} and Q_{p3} are always ON. Q_{p1} is driven by $\mathrm{PWM_A}$. Q_{p5} is driven by $\mathrm{PWM_B}$. Q_{p2} is always OFF. The body diode of Q_{p2} is reversely biased. The output capacitance of Q_{p2} (C_{oss}) is absorbed into the dc-link capacitor (C_A). The resonant current i_{r2} can only pass through two constant-ON switches, Q_{p3} and Q_{p4}. Since the voltage drop on the MOSFET channel is much lower than the voltage drop on the body diode, the conduction loss in the H5-bridge is reduced. On the other hand,

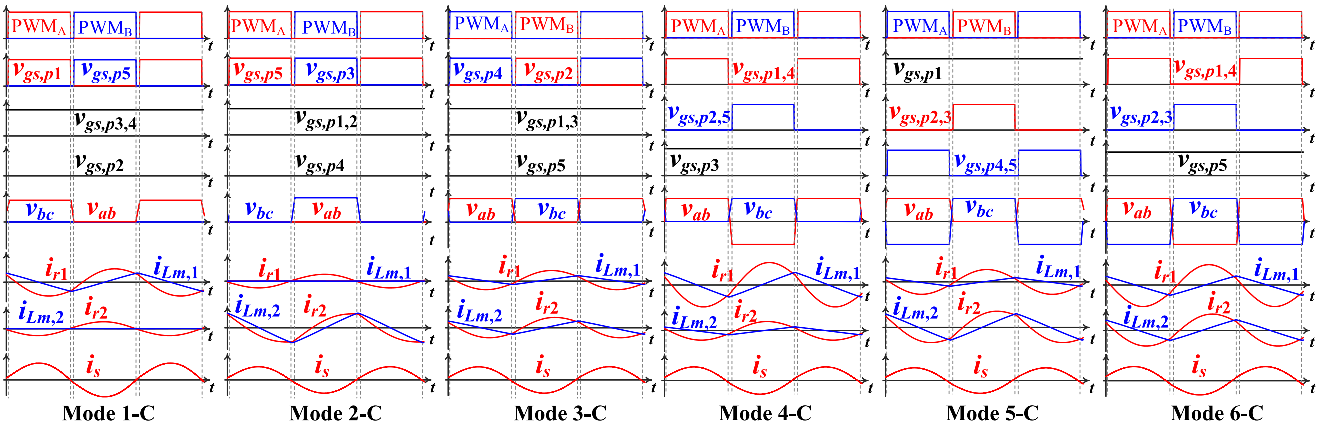


Fig. 2. Gate signals, v_{ab}, v_{bc}, and resonant current waveforms in the proposed reconfigurable DCX in the charging process (Modes 1-C–6-C).

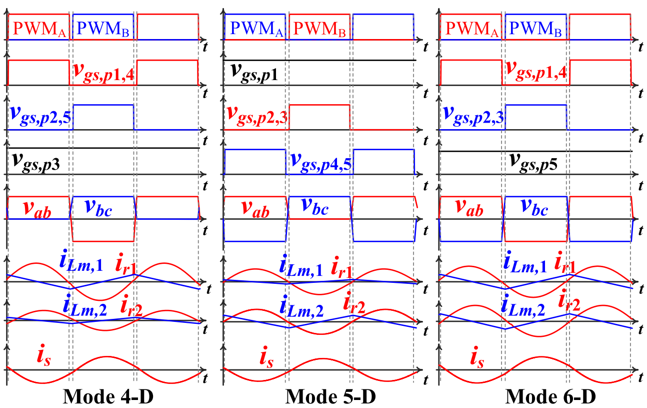


Fig. 3. Gate signals, v_{ab}, v_{bc}, and resonant current waveforms in the proposed reconfigurable DCX in the discharging process (Modes 4-D–6-D).

$v_{bc} = 0$. L_{m2} has a trivial voltage drop. Instant power through T_2 is nearly zero. v_{ab} is a square wave varying between 0 and $V_{\text{dc-link}}$.

This mode is equivalent to a $CLLC$ converter consisting of a half-bridge with RT1, T_1, and a full-bridge with RT3.

2) Mode 2-C: Q_{p1} and Q_{p2} are always ON. Q_{p5} is driven by PWM_A. Q_{p3} is driven by PWM_B. Q_{p4} is always OFF. The body diode of Q_{p4} is reversely biased. No current flows through it. The resonant current i_{r1} can only pass through two constant-ON switches, Q_{p1} and Q_{p2}. Moreover, $v_{ab} = 0$. L_{m1} has a trivial voltage drop. Instant power through T_1 is nearly zero. v_{bc} is a square wave varying between 0 and $V_{\text{dc-link}}$.

This mode is equivalent to a $CLLC$ converter consisting of a half-bridge with RT2, T_2, and a full-bridge with RT3. Since n_2 is smaller than n_1, the voltage conversion ratio $V_{\text{Bat}}/V_{\text{dc-link}}$ of Mode 2 is higher than that of Mode 1.

3) Mode 3-C: Q_{p1} and Q_{p3} are always ON. Q_{p5} is always OFF. Q_{p4} is driven by PWM_A. Q_{p2} is driven by PWM_B. v_{ab} and v_{bc} are square waves from 0 to $-V_{\text{dc-link}}$ with 180° phase shift.

This mode is equivalent to a $CLLC$ converter consisting of a half-bridge with RT1, T_1, a half-bridge with RT2, T_2, and a full-bridge with RT3. Due to the series-connected structure at the battery side, the voltage conversion ratio $V_{\text{Bat}}/V_{\text{dc-link}}$ of Mode 3 is higher than that of Mode 2.

4) Modes 4-C and 4-D: Q_{p3} is always ON. Q_{p1} and Q_{p4} are driven by PWM_A. Q_{p2} and Q_{p5} are driven by PWM_B. Port v_{ab} is a square wave from $-V_{\text{dc-link}}$ to $V_{\text{dc-link}}$. Port v_{bc} is a square wave from 0 to $V_{\text{dc-link}}$. v_{ab} and v_{bc} have 180° phase difference. v_{ab} works in the full-bridge mode and v_{bc} works in the half-bridge mode.

This mode is equivalent to a $CLLC$ converter consisting of a full-bridge with RT1, T_1, a half-bridge with RT2, T_2, and a full-bridge with RT3. Mode 4 has a higher voltage conversion ratio $V_{\text{Bat}}/V_{\text{dc-link}}$ than Mode 3.

5) Modes 5-C and 5-D: Q_{p1} is always ON. Q_{p4} and Q_{p5} are driven by PWM_A. Q_{p2} and Q_{p3} are driven by PWM_B. Port v_{ab} is a square wave from 0 to $V_{\text{dc-link}}$. Port v_{bc} is a square wave from $-V_{\text{dc-link}}$ to $V_{\text{dc-link}}$. v_{ab} and v_{bc} have 180° phase difference.

This mode is equivalent to a $CLLC$ converter consisting of a half-bridge with RT1, T_1, a full-bridge with RT2, T_2, and a full-bridge with RT3. Due to smaller n_2, the voltage conversion ratio $V_{\text{Bat}}/V_{\text{dc-link}}$ of Mode 5 is higher than that of Mode 4.

6) Modes 6-C and 6-D: Q_{p5} is always ON. Q_{p1} and Q_{p4} are driven by PWM_A. Q_{p2} and Q_{p3} are driven by PWM_B. v_{ab} and v_{bc} are square waves from $-V_{\text{dc-link}}$ to $V_{\text{dc-link}}$ with 180° phase difference.

This mode is equivalent to a $CLLC$ converter consisting of a full-bridge with RT1, T_1, a full-bridge with RT2, T_2, and a full-bridge with RT3. The voltage conversion ratio $V_{\text{Bat}}/V_{\text{dc-link}}$ in Mode 6 is the highest among all six modes.

III. Circuit Modeling and Gain Analysis

A. Circuit Modeling

The proposed converter has three resonant tanks, RT1, RT2, and RT3, as drawn in Fig. 4. u_1, u_2, and u_3 are the fundamental harmonic components of v_{ab}, v_{bc}, and v_{de}. Their root-mean-square (RMS) values are listed in Table I. If $V_{\text{dc-link}}$ is shorted ($u_1 = u_2 = 0$), the Thevenin equivalent impedance $Z_{o,s}$ seen

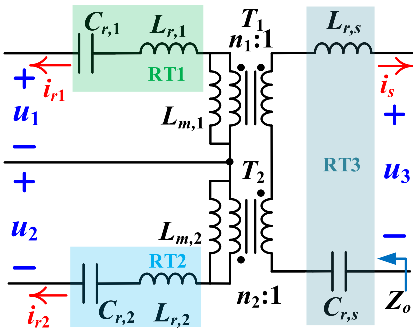


Fig. 4. Schematic of the resonant network.

TABLE I
RMS OF FUNDAMENTAL HARMONICS OF v_{ab}, v_{bc}, AND v_{de}

Configured Mode	u_1 RMS($v_{ab,1}$)	u_2 RMS($v_{bc,1}$)	u_3 RMS($v_{de,1}$)
Mode 1-C	$\sqrt{2}V_{\text{dc-link}}/\pi$	0	$2\sqrt{2}V_{Bat}/\pi$
Mode 2-C	0	$\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{Bat}/\pi$
Mode 3-C	$\sqrt{2}V_{\text{dc-link}}/\pi$	$\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{Bat}/\pi$
Mode 4-C, 4-D	$2\sqrt{2}V_{\text{dc-link}}/\pi$	$\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{Bat}/\pi$
Mode 5-C, 5-D	$\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{Bat}/\pi$
Mode 6-C, 6-D	$2\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{\text{dc-link}}/\pi$	$2\sqrt{2}V_{Bat}/\pi$

from port u_3 is

$$Z_{o,s} = sL_{r,s} + \frac{1}{sC_{r,s}} + \frac{s^2L_{m,1}L_{r,1}/n_1^2 + 1/(sC_{r,1})}{sL_{m,1} + sL_{r,1} + 1/(sC_{r,1})} + \frac{s^2L_{m,2}L_{r,2}/n_2^2 + 1/(sC_{r,2})}{sL_{m,2} + sL_{r,2} + 1/(sC_{r,2})}. \quad (1)$$

If port u_3 is open circuit, $i_s = 0$. The Thevenin equivalent source $u_{3,o}$ seen from port u_3 can be found

$$u_{3,o} = \frac{sL_{m,1}/n_1}{s(L_{m,1} + L_{r,1}) + 1/(sC_{r,1})}u_1 + \frac{sL_{m,2}/n_2}{s(L_{m,2} + L_{r,2}) + 1/(sC_{r,2})}u_2. \quad (2)$$

A unified circuit model can be derived by inverting the transform in Table I.

$$Z_{\text{th}} = \frac{\pi^2}{8}Z_{o,s}, \; V_{\text{th}} = \frac{\sqrt{2}\pi}{4}u_{3,o}. \quad (3)$$

The normalized switching frequency is $f_n = f_s/f_r$. $L_{n,1} = L_{m,1}/L_{r,1}$, $L_{n,2} = L_{m,2}/L_{r,2}$, $Z_{0,1} = \sqrt{L_{r,1}/C_{r,1}}$, $Z_{0,2} = \sqrt{L_{r,2}/C_{r,2}}$, $Z_{0,s} = \sqrt{L_{r,s}/C_{r,s}}$, and $s = j2\pi f_s$.

The unified equivalent impedance Z_{th} in Fig. 5 is

$$Z_{\text{th}}(f_n) = j\frac{\pi^2}{8}f_n(1-f_n^2)\left(\frac{1}{n_1^2}\frac{L_{n,1}Z_{0,1}}{1-f_n^2(1+L_{n,1})} + \frac{1}{n_2^2}\frac{L_{n,2}Z_{0,2}}{1-f_n^2(1+L_{n,2})} - \frac{Z_{0,s}}{f_n^2}\right). \quad (4)$$

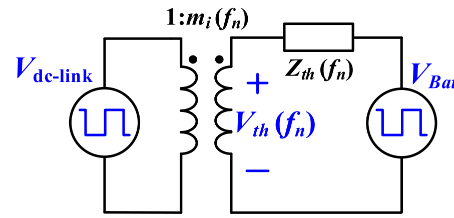


Fig. 5. Unified circuit model to describe six modes.

Six reconfigurable modes are modeled as an adjustable turns ratio transformer. Therefore, the analyses in charging and discharging processes are identical. The equivalent transformer turns ratio $m_i(f_n)$ in Mode i-C ($i = 1, 2, \ldots, 6$) and Mode i-D ($i = 4, 5, 6$) can be derived

$$m_i(f_n) = \frac{V_{\text{th}}(f_n)}{V_{\text{dc-link}}}, \quad i = 1, 2, 3, 4, 5, 6. \quad (5)$$

Make notation as

$$\psi_1(f_n) = \frac{-f_n^2L_{n,1}}{2n_1(1-f_n^2(1+L_{n,1}))} \quad (6)$$

$$\psi_2(f_n) = \frac{-f_n^2L_{n,2}}{2n_2(1-f_n^2(1+L_{n,2}))} \quad (7)$$

$$m_i = \begin{cases} \psi_1(f_n), & i=1 \\ \psi_2(f_n), & i=2 \\ \psi_1(f_n)+\psi_2(f_n), & i=3 \\ 2\psi_1(f_n)+\psi_2(f_n), & i=4 \\ \psi_1(f_n)+2\psi_2(f_n), & i=5 \\ 2\psi_1(f_n)+2\psi_2(f_n), & i=6 \end{cases}. \quad (8)$$

B. Gain Analysis

In the charging process, the battery can be modeled as an effective resistor

$$R_{l,\text{bat}} = \frac{V_{\text{Bat}}}{I_{\text{Bat}}}. \quad (9)$$

The output voltage can be calculated as

$$V_{\text{Bat}} = \left|\frac{R_{l,\text{bat}}}{R_{l,\text{bat}} + Z_{\text{th}}(f_n)}\right| V_{\text{th}}(f_n). \quad (10)$$

The forward voltage gain ($G_{p,i}$) in Mode i-C ($i = 1, 2, \ldots, 6$) is

$$G_{p,i} = \frac{V_{\text{Bat}}}{V_{\text{dc-link}}} = \left|\frac{R_{l,\text{bat}}}{R_{l,\text{bat}} + Z_{\text{th}}(f_n)}\right| m_i(f_n). \quad (11)$$

In the discharging process, the dc link can be modeled as an effective resistor

$$R_{l,\text{DC-link}} = \frac{V_{\text{dc-link}}}{I_{\text{dc-link}}}. \quad (12)$$

The output voltage can be derived similarly

$$V_{\text{dc-link}} = \left|\frac{R_{l,\text{dc-link}}m_i(f_n)}{R_{l,\text{dc-link}}m_i^2(f_n) + Z_{\text{th}}(f_n)}\right| V_{\text{Bat}}. \quad (13)$$

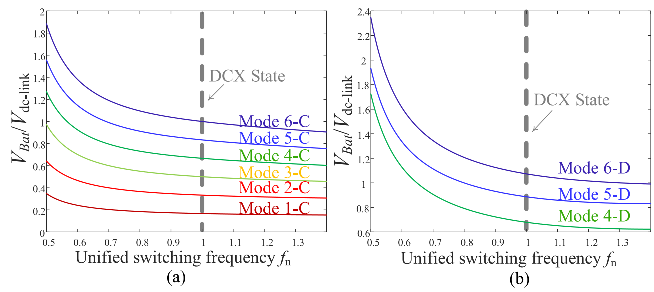


Fig. 6. Illustration of six modes' voltage gain curves in (a) charging and (b) discharging processes with $n_1 = 2n_2$.

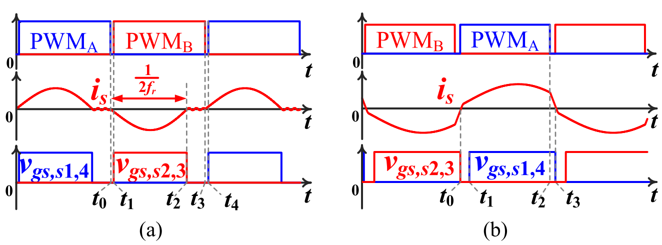


Fig. 7. SR waveforms (a) $f_s \leq f_r$ and (b) $f_s > f_r$ in the charging process.

The backward voltage gain ($G_{r,i}$) in Mode i-D ($i = 4, 5, 6$) is

$$G_{r,i} = \frac{V_{\text{dc-link}}}{V_{\text{Bat}}} = \left| \frac{R_{l,\text{dc-link}} m_i(f_n)}{R_{l,\text{dc-link}} m_i^2(f_n) + Z_{\text{th}}(f_n)} \right|. \quad (14)$$

According to (11)–(14), gain at the DCX state ($f_n = 1$) is only determined by n_1 and n_2. To make the gain curves distributed as an arithmetic sequence, the transformer ratios satisfy $n_1 = 2n_2$. The corresponding voltage gain curves are plotted in Fig. 6.

IV. SR Method for Bidirectional Operation

SR can improve the efficiency during the charging/discharging process due to less voltage drop on the MOSFET channel than the body diode. This section analyzes the SR method in conditions below, at, and above resonance for bidirectional operation.

A. Charging Process

The SR-gating signals in the charging process depend on the waveform of i_s, as demonstrated in Fig. 7.

1) Below and at Resonance ($f_s \leq f_r$): In Fig. 7(a), at t_0, PWM_A falls. i_s decreases from zero to negative. The negative i_s discharges the C_{oss} of $Q_{s2,3}$ and charges the C_{oss} of $Q_{s1,4}$.

During t_0–t_1, $i_{r,1}$ and $i_{r,2}$ are negative. With a proper deadband in PWM_A and PWM_B, ZVS can be achieved in the H5-bridge. At t_1, PWM_B is high and $v_{gs,s2,3}$ rises. The ZVS condition of Q_{s2} and Q_{s3} is established at t_1.

During t_0–t_2, $L_{r,s}$ resonates with $C_{r,s}$. At t_2, i_s reaches zero. Q_{s2} and Q_{s3} can achieve zero-current switching (ZCS) OFF. i_{r1} and i_{r2} fall on magnetizing currents $i_{Lm,1}$ and $i_{Lm,2}$. During the period t_2–t_3, Q_{s1}–Q_{s4} are all OFF. Due to $L_{m,1} \gg L_{r,1}$, $L_{m,2} \gg L_{r,2}$, $i_{r,1}$ and $i_{r,2}$ are nearly unchanged. Hence, i_s stays zero.

At t_3, PWM_B signal falls. The H5-bridge side enters into the deadband. At t_4, PWM_A rises. Body diodes of Q_{s1} and Q_{s4} conduct. Thus, a ZVS ON condition is created. Another half-cycle starts, similar to t_1–t_4.

Since an LC resonant tank RT3 sits on the battery side, the current in t_0–t_2 can be approximated as follows:

$$i_s(t) = -I_s \sin(2\pi f_r (t - t_0)). \quad (15)$$

In t_2–t_3, RT3 has no current; the averaged current in RT3 should be equal to the battery current

$$\left| \int_{t_0}^{t_3} i_s(t) dt \right| = \frac{I_{\text{Bat}} T_s}{2}. \quad (16)$$

The amplitude I_s can be derived

$$I_s = \frac{\pi}{2} I_{\text{Bat}} / f_n. \quad (17)$$

i_s needs to charge C_{oss} of the battery side

$$\left| \int_{t_0}^{t_1} i_s(t) dt \right| = 2 C_{oss} V_{\text{Bat}}. \quad (18)$$

The SR delay t_0–t_1 in the charging process is as follows:

$$t_1 - t_0 = \frac{1}{2\pi f_r} \arccos \left(\frac{I_{\text{Bat}} - 8 C_{oss} V_{\text{Bat}} f_s}{I_{\text{Bat}}} \right). \quad (19)$$

The conduction time (T_c) in Q_{s2} and Q_{s3} is

$$T_c = t_2 - t_1 = \frac{1}{2f_r} - \frac{1}{2\pi f_r} \arccos \left(\frac{I_{\text{Bat}} - 8 C_{oss} V_{\text{Bat}} f_s}{I_{\text{Bat}}} \right). \quad (20)$$

At light load, I_{Bat} is small. The upper limit of SR conduction time T_c is smaller than that in the normal load.

2) Above Resonance ($f_s > f_r$): In Fig. 7(b), at t_0, i_s reaches zero and goes to positive. It discharges C_{oss} of $Q_{s1,4}$ and charges C_{oss} of $Q_{s2,3}$. At t_1, $Q_{s1,4}$ are turned ON with ZVS. At t_2, PWM_A falls. $Q_{s1,4}$ conduct until t_3.

The fundamental harmonic component delivers the majority of power. From the former analysis, the phase between the H5-bridge and the battery-side bridge ($\phi_{SR,p}$) in the charging process is

$$\phi_{SR,p} = \text{angle} \left(\frac{R_{l,\text{bat}}}{R_{l,\text{bat}} + Z_{\text{th}}(f_n)} \right). \quad (21)$$

The phase shift is

$$t_3 - t_2 = \phi_{SR,p} / \omega_s = \frac{\phi_{SR,p}}{2\pi f_s}. \quad (22)$$

i_s during t_2–t_3 can be approximated as a triangle. Since f_s is near f_r, $\phi_{SR,p} \ll \pi$. The dead time of SR (t_d) can be calculated as

$$t_d = t_1 - t_0 = \frac{1}{2\pi f_r} \arccos \left(\frac{I_{\text{Bat}} - 8 C_{oss} V_{\text{Bat}} f_s}{I_{\text{Bat}}} \right). \quad (23)$$

At t_3, i_s reaches zero. Another half-cycle starts at t_3, just like t_0–t_3.

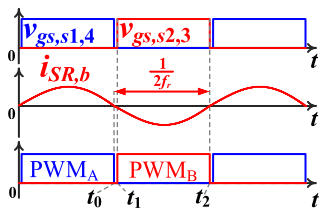


Fig. 8. SR waveforms $f_s = f_r$ in the discharging process.

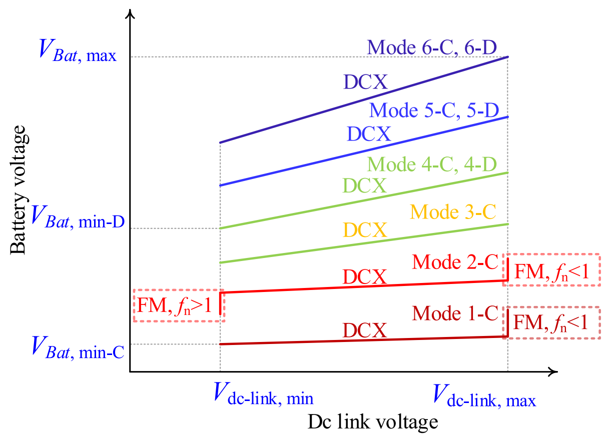


Fig. 9. Voltage range mapping between the battery and the dc link.

B. Discharging Process

Fig. 8 demonstrates the SR gating signals in the discharging process. In Mode i-D ($i = 4, 5, 6$), $f_s = f_r$. The SR signals are determined by the resonant currents flowing through $Q_{p2,4}$. Accordingly, mark the characteristic current as $i_{SR,b}$

$$i_{SR,b} = i_{Q_{p2}} = i_{Q_{p4}} = i_{r1} + i_{r2}. \tag{24}$$

At t_0, $i_{SR,b}$ reaches zero and goes to negative. It charges C_{oss} of the MOSFETs corresponding to $\mathrm{PWM_A}$ and discharges C_{oss} of the switches relevant to $\mathrm{PWM_B}$.

At t_1, $v_{gs,s2,3}$ rises. Meanwhile, body diodes of switches in relation with $\mathrm{PWM_B}$ conduct. $\mathrm{PWM_B}$ rises at t_1 so those switches can achieve ZVS ON.

At t_2, $v_{gs,s2,3}$ and $\mathrm{PWM_B}$ falls. $i_{SR,b}$ reaches zero. Another half-cycle starts, which is similar to the process of t_0–t_2. All MOSFETs in the H5-bridge can achieve ZVS ON and ZCS OFF. t_d can be calculated similarly to that in the charging process

$$t_d = t_1 - t_0 = \frac{1}{2\pi f_r} \arccos\left(\frac{I_{\text{dc-link}} - 8C_{oss}V_{\text{dc-link}}f_s}{I_{\text{dc-link}}}\right). \tag{25}$$

V. Design Considerations

Fig. 9 illustrates the voltage mapping of the proposed converter. In each reconfigurable mode, the dc-link voltage ranges from $V_{\text{dc-link,min}}$ to $V_{\text{dc-link,max}}$. It achieves an ultrawide battery voltage range from $V_{\text{Bat,min-C}}$ to $V_{\text{Bat,max}}$ for charging or $V_{\text{Bat,min-D}}$ to $V_{\text{Bat,max}}$ for discharging. As a result, the dc-link voltage span can be compressed compared with the conventional design. The overall f_s span is also squeezed. This section provides a perspective to design the continuous gain profile in adjacent modes.

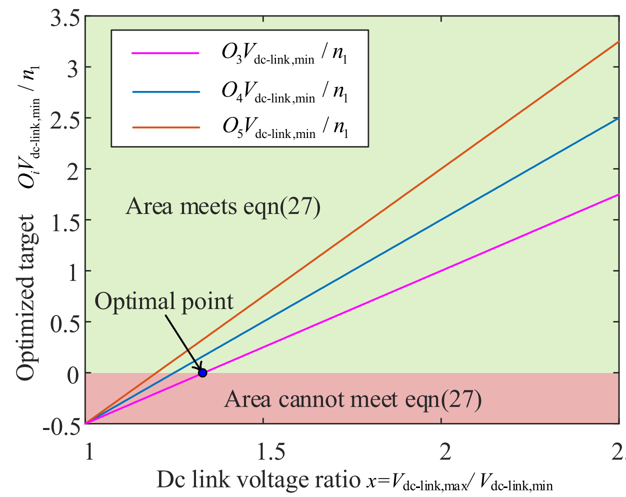


Fig. 10. Optimal design of dc-link side voltage.

A. Structural Design

To provide a continuous gain profile, the minimum battery voltage in mode $i + 1$ should be lower than the maximum battery voltage in mode i to avoid frequent mode transition at the critical points

$$\begin{aligned}
&i = 1, 2, 3, 4, 5 \text{ for the charging process}\\
&O_i = \max\left(G_{p,i}\right) \times V_{\text{dc-link,max}} -\\
&\qquad \min\left(G_{p,(i+1)}\right) \times V_{\text{dc-link,min}} \geq 0\\
&i = 4, 5 \text{ for the discharging process}\\
&O_i = \max\left(G_{r,i}\right) \times V_{\text{dc-link,max}} -\\
&\qquad \min\left(G_{r,(i+1)}\right) \times V_{\text{dc-link,min}} \geq 0.
\end{aligned} \tag{26}$$

To optimize the efficiency at heavy load conditions, in modes 4-C, 5-C, 6-C, and 4-D, 5-D, 6-D, the converter operates at the resonant frequency, where the voltage gain only depends on n_1 and n_2. Note that $y = n_1/n_2$ and $x = V_{\text{dc-link,max}}/V_{\text{dc-link,min}}$. This step is to find the optimal range of dc-link side voltage. To achieve the gain curves distributed as Fig. 6, $y = 2$. Therefore, (26) can be expressed as

$$\begin{aligned}
O_3 &= \left(\left(\frac{1}{2} + \frac{y}{2}\right)x - \left(1 + \frac{y}{2}\right)\right)\frac{n_1}{V_{\text{dc-link,min}}} \geq 0\\
O_4 &= \left(\left(1 + \frac{y}{2}\right)x - \left(\frac{1}{2} + y\right)\right)\frac{n_1}{V_{\text{dc-link,min}}} \geq 0\\
O_5 &= \left(\left(\frac{1}{2} + y\right)x - (1 + y)\right)\frac{n_1}{V_{\text{dc-link,min}}} \geq 0.
\end{aligned} \tag{27}$$

Fig. 10 plots the curves of the optimized target $O_iV_{\text{dc-link,min}}/n_1$ ($i = 3, 4, 5$) versus different x. The minimum x that makes all curves sit in the green area is optimal.

Therefore, $V_{\text{dc}-\text{link}} = 320$–420V. The continuous gain profile between modes 1-C, 2-C, and 3-C can be achieved with FM. Parameter design for that is given in the next paragraph.

B. Parameter Design

The transformer turns ratios n_1 and n_2 are also determined by $V_{\text{dc}-\text{link,max}}$ and $V_{\text{Bat,max}}$

$$V_{Bat,\max} = V_{\text{dc}-\text{link,max}}\left(\frac{1}{n_1} + \frac{1}{n_2}\right)$$
$$n_1 = 2n_2. \tag{28}$$

The gain curves are one, two, three, four, five, and six times the lowest one. For the case that $V_{\text{Bat,max}} = 420$ V, $n_1 = 3$ and $n_2 = 1.5$.

$L_{m,1}$ and $L_{m,2}$ need to provide the ZVS current for the MOSFETs of the inverter bridge during the dead time t_{dead}. Considering the worst case (Modes 1-C and 2-C)

$$L_{m,1} \leq t_{\text{dead}}/(16C_{oss}f_s),\ L_{m,2} \leq t_{\text{dead}}/(16C_{oss}f_s). \tag{29}$$

The ZVS current of Mode 1-C or 2-C is lower than that of other modes. Therefore, as long as the soft-switching conditions of these two modes are satisfied, ZVS in other modes can also be realized.

According to (11) and (14), the gain curves of the proposed converter are determined by four parameters $L_{n,1}, L_{n,2}, f_r, L_{r,s}$ besides f_n. The graphic method optimization is complicated. Therefore, parameter optimization uses the iterative method, as described in Fig. 11. The first step is to set f_r. Since $L_{m,1} \gg L_{r,1}$ and $L_{m,2} \gg L_{r,2}$, $L_{n,1}$ and $L_{n,2}$ iterate from their maximum value $L_{n1,\max}$ and $L_{n2,\max}$, respectively. Based on (4), the effect of $L_{r,s}$ on gain properties is opposite to that of $L_{n,1}$ and $L_{n,2}$. Hence, $L_{r,s}$ iterates from 0 to $L_{r,s,\max}$. The iteration ends if the range of operating f_n is limited in a predefined region $f_{n,\max} \geq f_n \geq f_{n,\min}$, where all six modes satisfy (26).

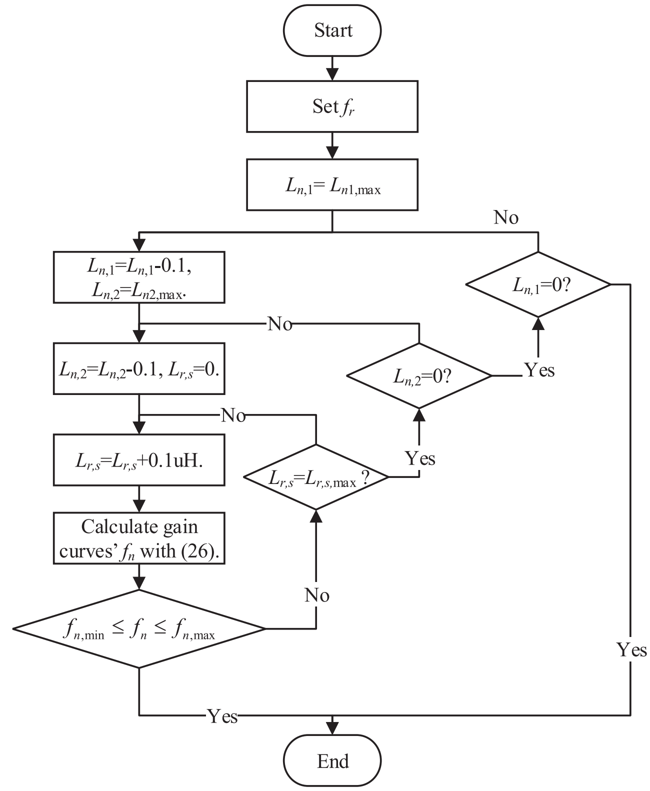


Fig. 11. Iterative parameter design.

C. Magnetic Design

The proposed converter works most of the time as DCX. Coefficients are noted as follows: the primary side turns number (n_p), the equivalent area of the core section (A_e), and the saturation flux (B_{sat}). At $f_s = f_r$, the flux variation in the transformer can be expressed as

$$\Delta B = \frac{V_{\text{dc}-\text{link,max}}}{4n_p A_e f_r} < B_{\text{sat}} \tag{30}$$

The transformer core loss (P_m) can be expressed with the Steinmetz equation [31]

$$P_m = V_c k f_r^{\alpha} \Delta B^{\beta} \tag{31}$$

where V_c is the core volume and k, α, and β are coefficients determined by the core material. The transformer winding loss (P_w) can be approximated by

$$P_w = I_p^2 R_{p,0}\left(M' + \frac{m_p^2 - 1}{3}D'\right)$$
$$+ (nI_p)^2 R_{s,0}\left(M' + \frac{m_s^2 - 1}{3}D'\right). \tag{32}$$

$R_{p,0}$ and $R_{s,0}$ are dc resistances of the transformer windings. $n = n_1$ or n_2 for T_1 or T_2, respectively. M' and D' are constant coefficients determined by the winding structure and skin depth. They are calculated with the Dowell method [32]. m_p and m_s are the layer numbers of primary and secondary windings, which depend on n_p and n. The currents in $L_{m,1}$ and $L_{m,2}$ are ignored for simplification. The transformer loss (P_{tr}) can be expressed as the sum of P_m and P_w:

$$P_{tr} = P_w + P_m. \tag{33}$$

Fig. 12 shows the total loss versus the primary winding turns number of both T_1 and T_2. The optimal winding numbers are $n_1 = 42 : 14$ and $n_2 = 42 : 28$.

D. Variable DC Link With Laddered DCX

A case study with 320–420 V dc-link voltage is conducted. The calculated $G_{p,i}$ and $G_{r,i}$ in the ultrawide charging voltage range and the wide discharging voltage range are listed in Table II. Hence, an ultrawide six times battery voltage range can be achieved.

The dc–dc stage works as DCX in Mode i-C $(i = 3, 4, 5, 6)$ and Mode i-D $(i = 4, 5, 6)$. FM is essential in Modes 1-C and 2-C to provide a connected output voltage range with Mode 3-C. The overall f_s band is squeezed.

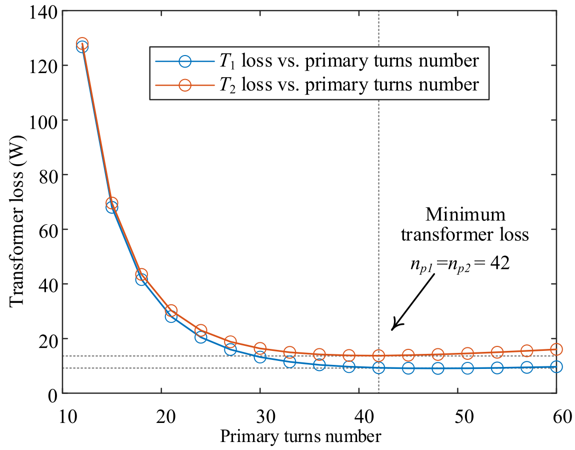


Fig. 12. Transformer loss P_{tr} versus primary turns number at $I_{\mathrm{Bat}} = 2.6$ A.

TABLE II
BATTERY VOLTAGE IN RECONFIGURABLE MODES IN 320–420-V DC-LINK CASE

Mode of H5-bridge	Region of switching frequency	Gains	Battery voltage range (V)
Mode 1-C	DCX	$G_{p,1} = 0.17$	$53 \sim 70$
	$f_s \leq f_r$ (at $V_{\mathrm{dc-link}} = 420\mathrm{V}$)	$G_{p,1} = 0.17 \sim 0.18$	$70 \sim 75$
Mode 2-C	$f_s \geq f_r$ (at $V_{\mathrm{dc-link}} = 320\mathrm{V}$)	$G_{p,2} = 0.23 \sim 0.33$	$75 \sim 106$
	DCX	$G_{p,2} = 0.33$	$106 \sim 140$
	$f_s \leq f_r$ (at $V_{\mathrm{dc-link}} = 420\mathrm{V}$)	$G_{p,2} = 0.33 \sim 0.38$	$140 \sim 160$
Mode 3-C	DCX	$G_{p,3} = 0.50$	$160 \sim 210$
Mode 4-C	DCX	$G_{p,4} = 0.66$	$210 \sim 280$
Mode 5-C	DCX	$G_{p,5} = 0.83$	$266 \sim 350$
Mode 6-C	DCX	$G_{p,6} = 1.00$	$320 \sim 420$
Mode 4-D	DCX	$G_{r,4} = 1.50$	$213 \sim 280$
Mode 5-D	DCX	$G_{r,5} = 1.20$	$266 \sim 350$
Mode 6-D	DCX	$G_{r,6} = 1.00$	$320 \sim 420$

The implementation of the controller is illustrated in Fig. 13. T_c in the below resonance region and $\phi_{SR,p}$ and t_d in the above resonance region are calculated for SR gating. In the charging process, constant current (CC) or constant voltage (CV) modes are selected to regulate the battery current or voltage. In the discharging process, the dc-link voltage is regulated. $T_{sc,0,k}$ and $T_{sd,0,k}$ are the corresponding minimum switching periods in mode k for the charging and discharging process, respectively. $\mathrm{PWM_A}$, $\mathrm{PWM_B}$, and SR gating signals are synchronized via the same sawtooth wave carrier signal. Mode k is selected according to Table II. The reconfigurable switch pattern gating can be implemented using a multiplexer (MUX).

The mode transient is activated if V_{Bat} reaches the hysteretic boundary. Then, the configuration of the MUX is updated when the sawtooth carrier reaches zero. The proportional–integral (PI) controller is also updated to regulate the output voltage. In synergy with the variable dc-link framework, the switching frequency will be constrained to the vicinity of the resonant frequency.

The gain range of a specific operating mode depends on (11) and (14). However, with the variable dc-link framework, the switching frequency of the proposed converter is always in the DCX state in modes 3-C, 4-C(-D), 5-C(-D), and 6-C(-D). The gain in these mode only depends on the transformer turns ratio n_1 and n_2. In Modes 1-C and 2-C, the gain ranges are decoupled. Therefore, the component mismatch in mode selection can be tolerated.

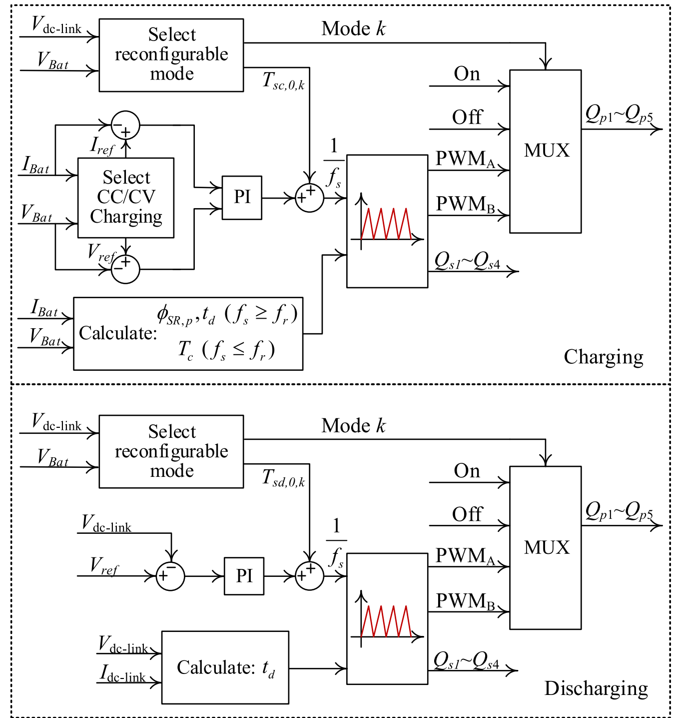


Fig. 13. Control diagrams in charging and discharging processes.

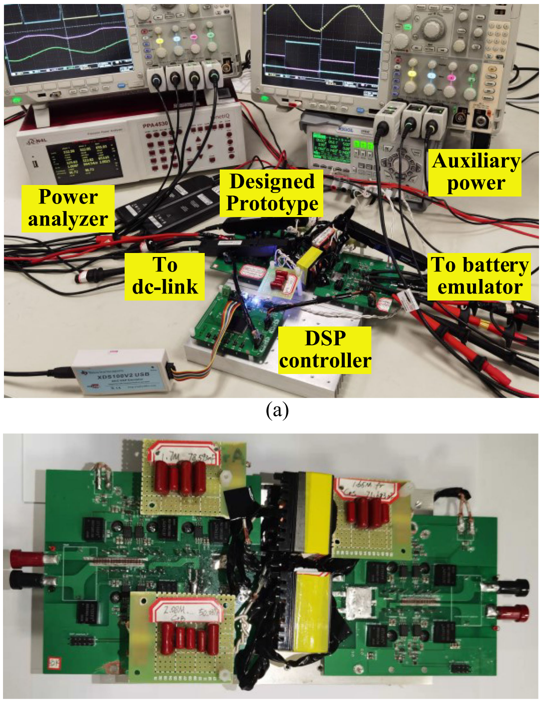
TABLE III
DESIGN PARAMETERS

Symbol	Quantity	Parameters
$V_{\mathrm{dc-link}}$	Dc-link voltage	$320\mathrm{V} \sim 420\mathrm{V}$
V_{Bat}	Charging battery voltage Discharging battery voltage	$55\mathrm{V} \sim 420\mathrm{V}$ $230\mathrm{V} \sim 420\mathrm{V}$
$L_{r,1}, L_{r,2}, L_{r,s}$	Resonant inductance	44.7μH, 70μH, 49μH
$C_{r,1}, C_{r,2}, C_{r,s}$	Resonant capacitance	78nF, 50nF, 71.5nF
$L_{m,1}, L_{m,2}$	Magnetizing inductance	516.3μH, 516.9μH
n_1, n_2	Transformer turns ratio	42:14, 42:28
$Q_{s,1\sim4}, Q_{p,1\sim5}$	MOSFET switch	SCT3120AL
T_1, T_2	Transformer core	PC95 EER42/42/20

VI. EXPERIMENTAL RESULTS

To verify the proposed concept, a 1-kW rated prototype with 320–420 V dc link is tested, as shown in Fig. 14. It validates 55–420 V charging voltage and 230–420 V discharging voltage for the battery side.

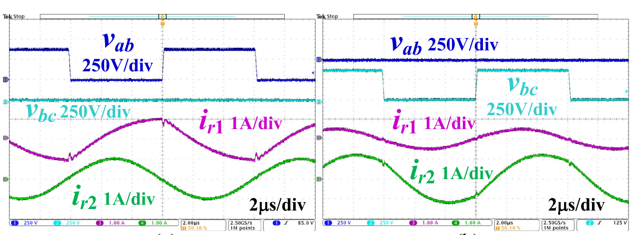
The specifications and prototype parameters are listed in Table III. The leakage inductance of transformers implements the resonant inductance. A metalized polypropylene film capacitor



(a)

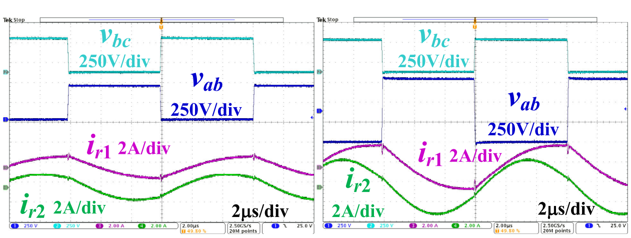
(b)

Fig. 14. (a) Experimental setup. (b) Designed prototype.



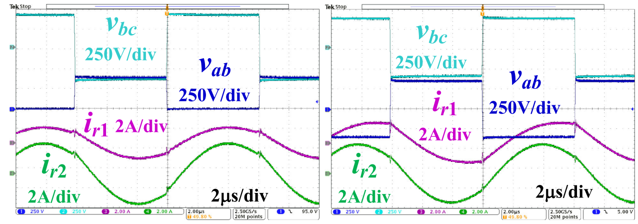
(a) (b)

Fig. 15. Steady-state waveforms in (a) Mode 1-C with $V_{\mathrm{dc-link}} = 380$ V and $I_{\mathrm{Bat}} = 1$ A and (b) Mode 2-C with $V_{\mathrm{dc-link}} = 360$ V and $I_{\mathrm{Bat}} = 1$ A.



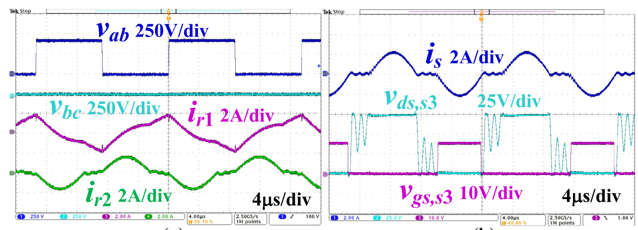
(a) (b)

Fig. 16. Steady-state waveforms in (a) Mode 3-C with $V_{\mathrm{dc-link}} = 400$ V and $I_{\mathrm{Bat}} = 1$ A and (b) Mode 4-C with $V_{\mathrm{dc-link}} = 360$ V and $I_{\mathrm{Bat}} = 2.6$ A.



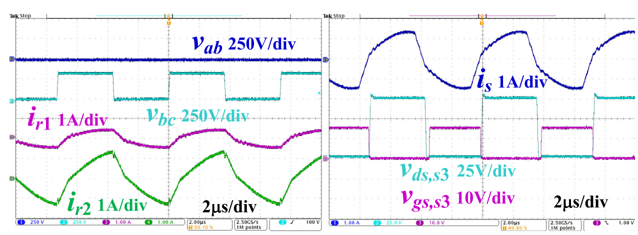
(a) (b)

Fig. 17. Steady-state waveforms in (a) Mode 5-C with $V_{\mathrm{dc-link}} = 400$ V and $I_{\mathrm{Bat}} = 2.6$ A and (b) Mode 6-C with $V_{\mathrm{dc-link}} = 360$ V and $I_{\mathrm{Bat}} = 2.6$ A.



(a) (b)

Fig. 18. Steady-state waveforms in Mode 1-C, $f_s < f_r$, $V_{\mathrm{dc-link}} = 420$ V, and $I_{\mathrm{Bat}} = 1$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.



(a) (b)

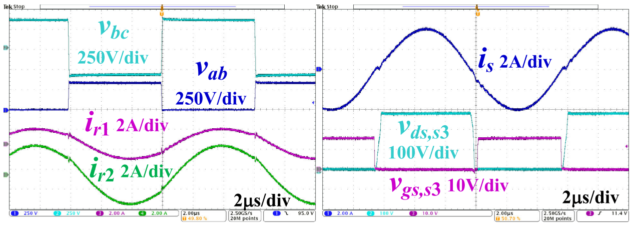
Fig. 19. Steady-state waveforms in Mode 2-C, $f_s > f_r$, $V_{\mathrm{dc-link}} = 320$ V, and $I_{\mathrm{Bat}} = 1$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.

is selected as the resonant capacitors. The proposed converter works in the variable dc-link framework. In Modes 1-C and 2-C, FM is adopted. In Mode i-C ($i = 3, 4, 5, 6$) and Mode i-D ($i = 4, 5, 6$), the proposed converter works at the DCX state ($f_s = f_r = 82$ kHz).

Figs. 15–17 capture the proposed H5-bridge reconfiguration strategy waveforms in the charging process. In Fig. 15, $v_{bc} = 0$ in Mode 1-C and $v_{ab} = 0$ in Mode 2-C. Single half-bridge v_{ab} (Mode 1-C) and single half-bridge v_{bc} (Mode 2-C) are verified. The proposed strategy can eliminate the body diode conduction with reverse bias. Moreover, the average power delivered by the idle resonant tank is zero. No real power is transferred through it. Besides, the resonant current in the idle resonant tank is in phase with the port voltage of the active resonant tank. Conduction loss in the idle resonant tank is reduced.

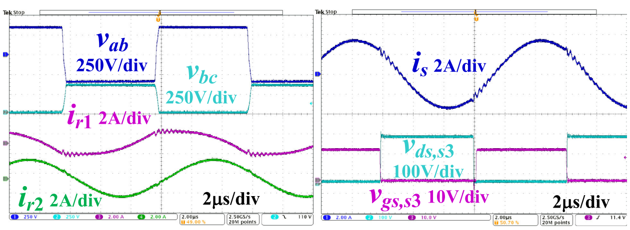
In Figs. 16 and 17, a phase difference in i_{r1} and i_{r2} occurs. It relates with the load distribution between transformers T_1 and T_2. Dual half-bridge (Mode 3-C), full-bridge v_{ab} half-bridge v_{bc} (Mode 4-C), half-bridge v_{ab} full-bridge v_{bc} (Mode 5-C), and dual full-bridge (Mode 6-C) are verified.

Figs. 18–20 demonstrate the performance of the proposed SR method in the charging process. In Modes 1-C and 2-C, FM is used to make the voltage gain range continuous. At the maximum dc-link voltage, Modes 1-C and 2-C work in the below



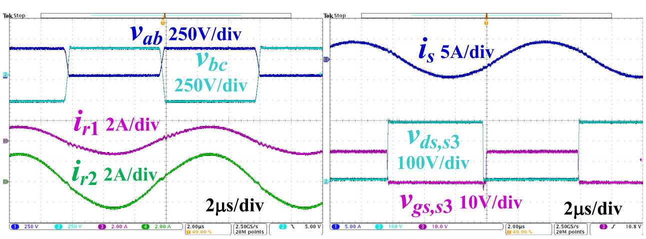
(a) (b)

Fig. 20. Steady-state waveforms in Mode 5-C, $f_s = f_r$, $V_{\text{dc-link}} = 340$ V, and $I_{\text{Bat}} = 1$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.



(a) (b)

Fig. 21. Steady-state waveforms in Mode 4-D, $V_{\text{dc-link}} = 340$ V and $I_{\text{Bat}} = 1.70$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.

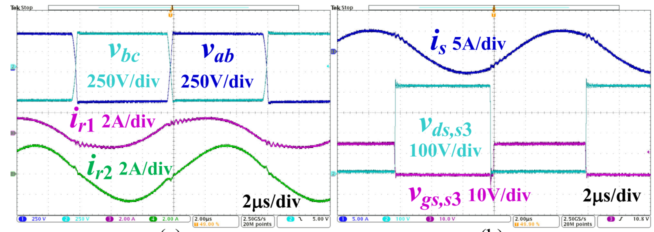


(a) (b)

Fig. 22. Steady-state waveforms in Mode 5-D, $V_{\text{dc-link}} = 327$ V and $I_{\text{Bat}} = 2.52$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.

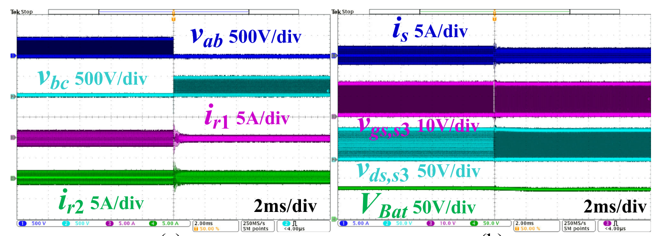
f_r region. Fig. 18 captures the Mode 2-C steady-state waveform at $f_s < f_r$. At the minimum dc-link voltage, Modes 1-C and 2-C work in the region above f_r. Fig. 19 captures the steady-state waveform of Mode 2-C at $f_s > f_r$. In Mode i-C $(i = 3, 4, 5, 6)$, the converter works in the DCX state. The SR method works at the resonant point. Fig. 20 captures the Mode 5-C steady-state waveform. The proposed SR method achieves ZVS ON and ZCS OFF of the battery-side full-bridge in the charging process.

In Mode i-D $(i = 4, 5, 6)$, the prototype works at the DCX state. Figs. 21–23 show the captured waveforms. Q_{s3} achieves ZVS ON. Due to symmetrical gating, the battery-side full-bridge can achieve ZVS ON. Port v_{ab} and port v_{bc} change the polarity near $i_{r1} + i_{r2}$ zero crossing point. The proposed SR method achieves ZVS ON and ZCS OFF of the H5-bridge in the discharging process. Fig. 21 demonstrates that the H5-bridge forms a full-wave rectifier v_{ab} and a voltage doubler v_{bc}. In Fig. 22, port v_{bc} works as a full-wave rectifier, while port v_{ab} works as a voltage doubler. Both v_{bc} and v_{ab} are configured as full-wave rectifiers in Fig. 23.



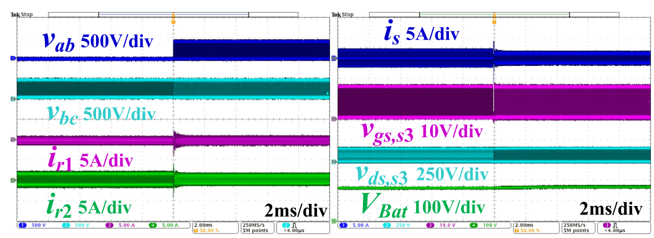
(a) (b)

Fig. 23. Steady-state waveform in Mode 6-D, $V_{\text{dc-link}} = 410$ V and $I_{\text{Bat}} = 2.52$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.



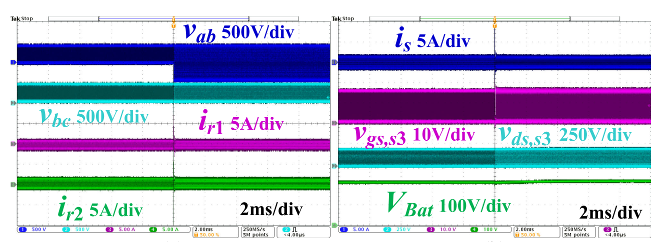
(a) (b)

Fig. 24. Transition from Mode 1-C to Mode 2-C, $V_{\text{dc-link}} = 420$ V and $I_{\text{Bat}} = 1$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.



(a) (b)

Fig. 25. Transition from Mode 2-C to Mode 3-C, $V_{\text{dc-link}} = 420$ V and $I_{\text{Bat}} = 1$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.



(a) (b)

Fig. 26. Transition from Mode 3-C to Mode 4-C, $V_{\text{dc-link}} = 420$ V and $I_{\text{Bat}} = 1$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.

The experimental results of mode transitions in the charging process are captured in Figs. 24–28. During the transition, the SR is disabled for several switching periods to avoid potential shoot-through, as shown in panel (b) in Figs. 24–28. Then, the switching frequency is stepped up to maintain a continuous voltage gain. In 400 μs, the new steady state is achieved, and the SR is enabled. As shown, the battery-side voltage is stable during this process, which indicates a smooth transition.

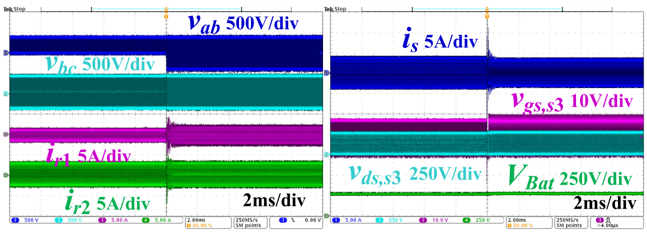


Fig. 27. Transition from Mode 4-C to Mode 5-C, $V_{\mathrm{dc-link}} = 400$ V and $I_{\mathrm{Bat}} = 2.6$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.

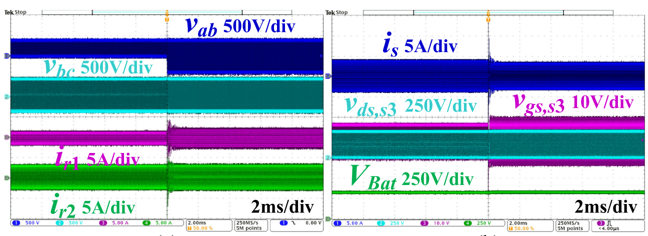


Fig. 28. Transition from Mode 5-C to Mode 6-C, $V_{\mathrm{dc-link}} = 390$ V and $I_{\mathrm{Bat}} = 2.6$ A. (a) H5-bridge waveforms. (b) Battery-side full-bridge waveforms.

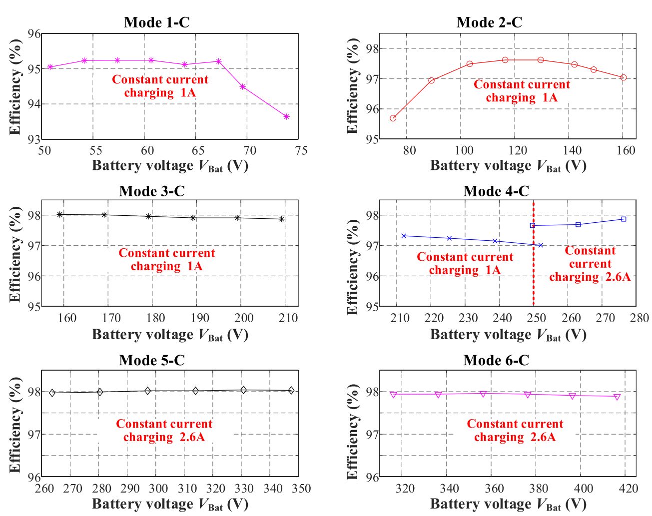


Fig. 29. Measured efficiency in the CC charging state.

Fig. 29 shows the measured efficiency in the CC charging state. Below $V_{\mathrm{Bat}} = 250$ V is the precharging CC zone ($I_{\mathrm{pre}} = 1$ A). $V_{\mathrm{Bat}} = 250$–420 V is the normal CC charging zone ($I_{\mathrm{chg}} = 2.6$ A). Under an ultrawide voltage range, the proposed converter achieves high efficiency. The measured peak efficiency is 98.04%. The efficiency is close to each other at the same CC condition in the DCX state (Mode i-C $(i = 3, 4, 5, 6)$). Due to FM in Modes 1-C and 2-C, the efficiency drops when f_s deviates from f_r. Compared with the conventional design in [12], the efficiency is improved in the entire CC charging range.

Fig. 30 presents the measured efficiency in the CV charging mode. The battery current varies from 0.2 to 2.6 A. The measured peak charging efficiency in this range is 97.89%. The major loss

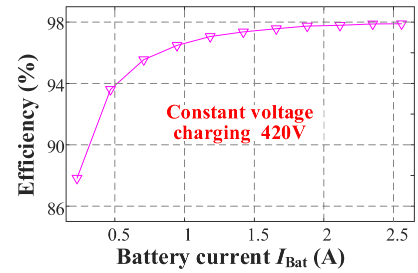


Fig. 30. Measured efficiency in the CV charging state in Mode 6-C.

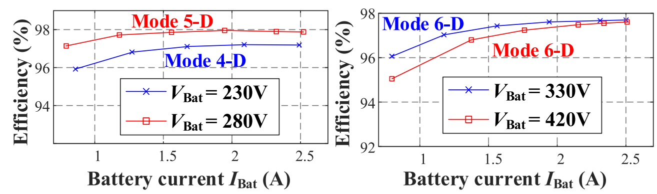


Fig. 31. Measured efficiency in the discharging state under different battery voltage levels.

at light-load condition consists of magnetic loss and circulating loss that are load independent. Therefore, the proportion of major loss in the delivered power increases as the load decreases, which jeopardizes the light-load efficiency [33].

Fig. 31 exhibits the measured efficiency curves in the discharging process with 230–420 V battery voltage. High efficiency is provided over different battery voltage levels. The peak measured efficiency is 97.96% in the discharging process.

VII. Conclusion

In this article, a novel H5-bridge-based $CLLC$ resonant converter was proposed for PEV charging applications. The H5-bridge is bidirectionally reconfigurable. Therefore, two resonant tanks could provide six modes in the charging process and three modes in the discharging process. Gain curves can be distributed in an arithmetic sequence. With the proposed H5-bridge reconfiguration strategy as well as the variable dc-link framework, the operating frequency is near $f_n = 1$. Hence, the efficiency is effectively improved in the bidirectional wide gain range. Moreover, the span of dc-link voltage is squeezed. The operating principles, circuit modeling, and SR method are detailed.

To validate the proposed concept, a 1-kW rated prototype is tested. The tested prototype achieves 55–420 V charging voltage and 230–420 V discharging voltage with a 320–420 V dc link. A 98.02% peak efficiency and a good efficiency over the bidirectional wide voltage range are recorded.

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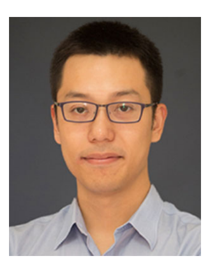

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