

A SiC-Based Highly Integrated Bidirectional AC/DC Converter for PEV Charging Applications

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Abstract—High power density with low hardware cost is one of the driving forces in the evolution of plug-in electric vehicles (PEVs) onboard chargers. To achieve this target, this paper proposes a highly integrated ac/dc converter for PEV charging applications. In the proposed structure, a single-phase bidirectional totem-pole power-factor-correction (PFC) converter is implemented mainly using the existing components in the driving system. The motor drive and windings are reused as switches and inductors, respectively. Therefore, the hardware cost of the onboard charger is significantly reduced. SiC semiconductors are employed to resolve the reverse recovery issues. The proposed converter is featured with reduced components count, reduced input current ripples, and bidirectional power flow. Circuit analysis and design considerations are detailed. A 500 W bidirectional ac/dc converter prototype is designed and tested to verify the concept.

Keywords—Bidirectional, PEV charging, SiC, totem pole.

I. INTRODUCTION

To charge the onboard battery pack of the plug-in electric vehicles (PEVs), an ac/dc converter is required in the onboard charger [1]–[4]. This converter rectifies the grid-side ac voltage to a dc voltage on the dc link and maintains a unity power factor. Generally, high power density and low hardware cost are among the major desired features in designing this ac/dc converter. For vehicle-to-grid (V2G) enabled onboard chargers, bidirectional power flow is also required [5]. However, in conventional bridged ac/dc converters, the diode loss is substantial [6], [7]. Therefore, bridgeless Boost and its derived topologies are the emerging technology utilized in this ac/dc PFC converter [8].

Among bridgeless boost topologies, totem-pole ac/dc maintains the lowest components count, exhibits low common-mode noise, and can achieve bidirectional power flow [8]. However, it suffers from severe reverse recovery issues in continuous conduction mode induced by silicon MOSFETs [9]. While deploying SiC power MOSFETs could effectively mitigate this issue. Thus, recent progress in commercialized wide band-gap power semiconductors revitalizes the bridgeless totem-pole PFC topology in various applications [10], [11].

On the other hand, topology reuse enhances the power density and reduces the hardware cost of the PEV onboard charger. Fig. 1 shows the typical powertrain of the PEV with the regenerative braking feature. Recently, the concept of an integrated charger has drawn intensive research attention. In [12], a multifunctional onboard PEV battery charger is proposed. The full-bridge in the front-end ac/dc PFC converter is reused as the bidirectional dc/dc converter, which links the auxiliary battery into the dc bus. In [13], a three-phase onboard charger that is integrated with the propulsion

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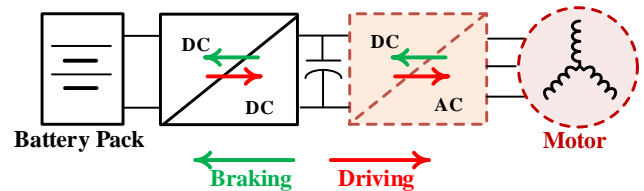


Fig. 1. Block diagram of the PEV powertrain.

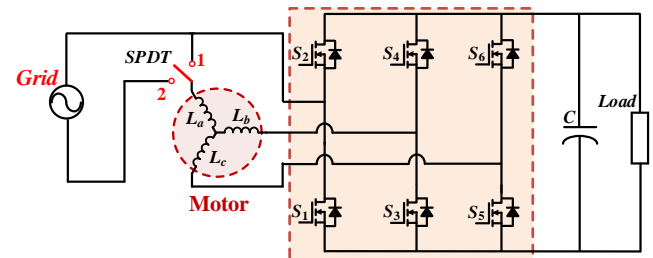


Fig. 2. Schematic of the proposed integrated bidirectional ac/dc converter.

system of PEV is presented. It is constructed by connecting an add-on three-phase power electronic interface to the propulsion system. In [14], a bidirectional dc/dc converter is proposed to be reused both in the charging and driving modes. In [15], a bidirectional onboard charger integrated with the accessory power converter is proposed. The segmented traction drive system is utilized as the front-end converter. In [16], two traction drive systems are series-connected to act as the front end ac/dc. An inductor-diode circuit is introduced to reduce the common-mode noise. In [17], a high voltage battery-powered dual traction drive system is utilized to realize the front-end stage with a programmable power factor to generate real and reactive power. Generally, the hardware of the powertrain can be reused in the onboard charging system with the integrated chargers. Therefore, the system power density can be further enhanced.

In this paper, a highly integrated ac/dc converter is proposed for PEV charging systems. The schematic of the proposed converter is plotted in Fig. 2. The switches of the three-phase bridge in the motor drive are reused in the interleaved totem-pole Boost PFC converter, while the windings of the permanent magnet synchronous motor are reused as the inductors. The proposed integrated ac/dc PFC converter has the following advantages: a) reverse recovery issues mitigated by the SiC semiconductors, b) minimized components count with the highest level of integration, c) canceled input current ripples due to the interleaving structure, d) improved common-mode noise with totem-pole configuration, and e) bidirectional power flow.

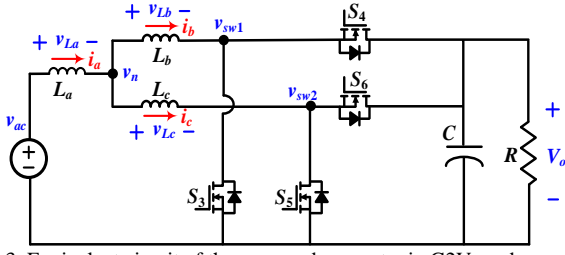


Fig. 3. Equivalent circuit of the proposed converter in G2V mode.

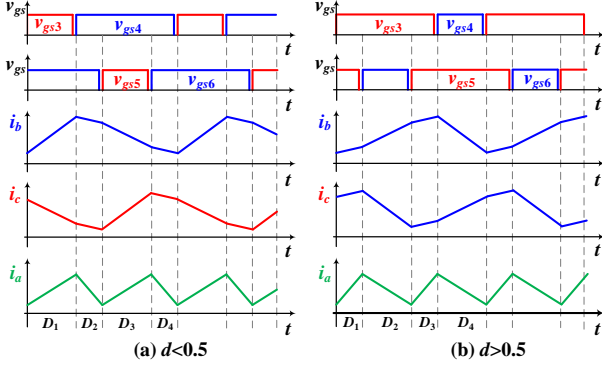


Fig. 4. Steady-state waveforms in ac/dc PFC operation.

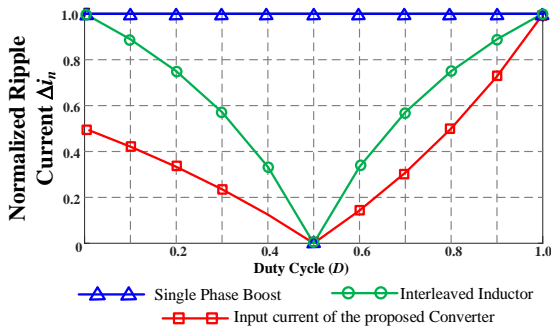


Fig. 5. Effective input current ripple cancellation effect.

II. OPERATION PRINCIPLE AND ANALYSIS

The proposed ac/dc converter aims to realize the bidirectional power flow between the grid and the intermediate dc bus while fully relying on the drivetrain modules. A single-pole-double-throw switch is added to facilitate function transition between PFC and motor drive. When the pole is in position 1, the converter acts as a motor drive. When the pole is triggered to throw 2, charging mode is enabled. Half-bridge S_1 - S_2 is switched at the grid frequency and collaborates with the grid-side polarity detector. Full bridge S_3 - S_6 functions as the boost switches and is switched at the switching frequency (f_s). For the convenience of discussion, only the positive half-period is analyzed. The negative half-period is similar.

In grid-to-vehicle mode, the equivalent circuit of the proposed ac/dc converter is plotted in Fig. 3. A 180° phase shift is enforced between switching actions of half-bridges S_3 - S_4 and S_5 - S_6 . The driving pattern and the key steady-state waveforms are illustrated in Fig. 4. Due to the motor winding symmetry, $L_a = L_b = L_c$. Apply Kirchhoff's current law on node v_n , $i_a = i_b + i_c$. Therefore, the voltage of v_n and L_a can be derived in (1-2). T_s is the switching period.

$$v_n = \frac{v_{ac} + v_{sw1} + v_{sw2}}{3}, \quad (1)$$

$$v_{L_a} = \frac{2v_{ac} - v_{sw1} - v_{sw2}}{3}. \quad (2)$$

Since v_{sw1} and v_{sw2} have 180° phase shift, v_n changes twice in a switching period. Thus, $D_1 = D_3$ and $D_2 = D_4$. The current ripple frequency of i_a is strictly equals $2f_s$. Consider the volt-second λ on L_a :

$$\lambda = \begin{cases} \frac{2v_{ac} - v_o}{3}d + \frac{2v_{ac} - 2v_o}{3}(0.5 - d), & d < 0.5 \\ \frac{2v_{ac} - v_o}{3}(1 - d) + \frac{2v_{ac}}{3}(d - 0.5), & d \geq 0.5 \end{cases} \quad (3)$$

With the volt-second balance, the dc gain is derived in (4).

$$G = \frac{v_o}{v_{ac}} = \frac{1}{1 - d}. \quad (4)$$

According to (3), the input current ripple is in (5).

$$\Delta i_{in} = \Delta i_a = \begin{cases} \frac{v_o(1 - 2d)dT_s}{6L}, & d < 0.5 \\ \frac{v_o(1 - d)(2d - 1)T_s}{6L}, & d \geq 0.5 \end{cases} \quad (5)$$

Similarly, the ripple current on inductor L_b and L_c can also been derived in (6).

$$\Delta i_b = \Delta i_c = \begin{cases} \frac{v_o(2 - d)dT_s}{6L}, & d < 0.5 \\ \frac{v_o(1 - d^2)T_s}{6L}, & d \geq 0.5 \end{cases} \quad (6)$$

Compared with the single phase boost situation whose ripple current is shown in (7).

$$\Delta i_{sp} = \frac{d(1 - d)T_s}{L} v_o. \quad (7)$$

The normalized ripple current is defined as follows. For interleaved boost inductors L_b and L_c , the normalized ripple current $\Delta i_{n,bc}$ is in (8). For the input current, $\Delta i_{n,in}$ is shown in (9).

$$\Delta i_{n,bc} = \Delta i_c / \Delta i_{sp} = \Delta i_b / \Delta i_{sp} = \begin{cases} \frac{(1 - 2d)}{2 - d}, & d < 0.5 \\ \frac{(2d - 1)}{2 - d}, & d \geq 0.5 \end{cases} \quad (8)$$

$$\Delta i_{n,in} = \Delta i_a / \Delta i_{sp} = \begin{cases} \frac{(1 - 2d)}{1 - d}, & d < 0.5 \\ \frac{(2d - 1)}{d}, & d \geq 0.5 \end{cases} \quad (9)$$

In comparison with the conventional single-phase Boost PFC and two-phase interleaved Boost PFC converters, the input current of the proposed converter can be reduced. This ripple cancellation effect is plotted in Fig. 5.

To achieve a unity power factor, the average input current can be derived as (10).

$$I_{in} = \frac{V_o^2}{Rv_{ac}(t)} = \frac{V_o}{R(1-d)}. \quad (10)$$

The maximum and minimum current of the proposed converter can be derived in (11-12).

$$I_{in,max} = \begin{cases} \frac{V_o}{R(1-d)} + \frac{(1-2d)v_o}{6L} dT_s, & d < 0.5 \\ \frac{V_o}{R(1-d)} + \frac{(2d-1)v_o(1-d)T_s}{6L}, & d \geq 0.5 \end{cases} \quad (11)$$

$$I_{in,min} = \begin{cases} \frac{V_o}{R(1-d)} - \frac{(1-2d)v_o}{6L} dT_s, & d < 0.5 \\ \frac{V_o}{R(1-d)} - \frac{(2d-1)v_o(1-d)T_s}{6L}, & d \geq 0.5 \end{cases} \quad (12)$$

Accordingly, the components current stresses can be evaluated based on the current ripple and average current.

III. CONTROL STRATEGY

The proposed converter deploys a dedicated control strategy to regulate the output voltage, suppress the total harmonic distortion (THD), and ensure a high power factor. The utilized control strategy in ac/dc PFC mode is illustrated in Fig. 6. There are two PI compensation loops. The inner loop regulates the input current and power factor. The outer loop regulates the dc-link voltage.

A digital phase-locked loop (PLL) with zero detection and counter is used to obtain a standard sinusoidal signal with the same frequency and phase information from the grid voltage. Using this signal as a reference, we can eliminate the sensing noise induced by switching devices, reduce THD, and improve the system power factor.

The output voltage is compared with the reference voltage. The difference passes through the PI compensator of the voltage loop to get the equivalent admittance seen from the grid. It is multiplied by the standard sinusoidal signal $v_{in,ref}$ to generate the current reference. The present averaged input current is compared with the current reference and feed the result into the inner loop PI compensator to generate the applied duty cycle.

In summary, the amplitude of the averaged input current reference is adjusted to meet the required voltage output. Correspondingly, the output duty cycle will change to achieve a sinusoidal current signal.

IV. SIMULATION RESULTS

To verify the feasibility of the proposed concepts, this work simulates the closed-loop system. The simulation parameters are as follows: the input voltage is 220 Vrms, 60 Hz. The output voltage is 450 Vdc, and the delivered power is 500W. f_s is 50 kHz. The sampling frequency and control frequency of the closed-loop system is the same as f_s .

The closed-loop simulation is shown in Fig. 7. The input voltage is in phase with the input current. The power factor is approximately equal to one. Fast Fourier transform (FFT) analysis of the input current is shown in Fig. 8. The THD of the input current is 2.67%.

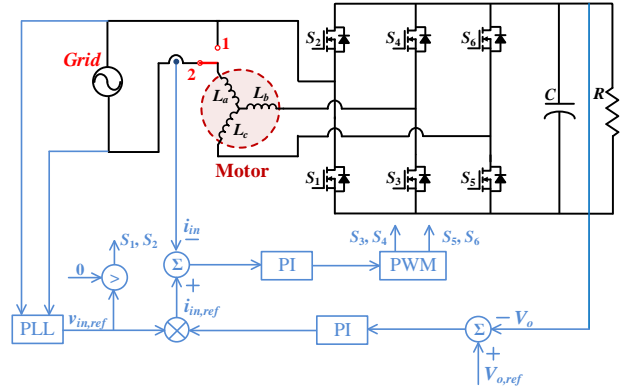


Fig. 6. Block diagram of the utilized control strategy in ac/dc PFC mode.

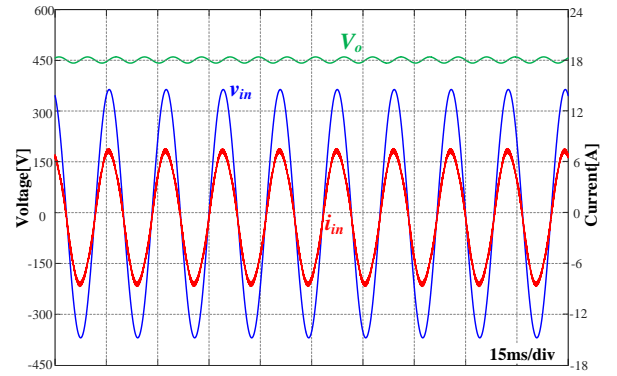


Fig. 7. Simulated waveforms in ac/dc PFC mode.

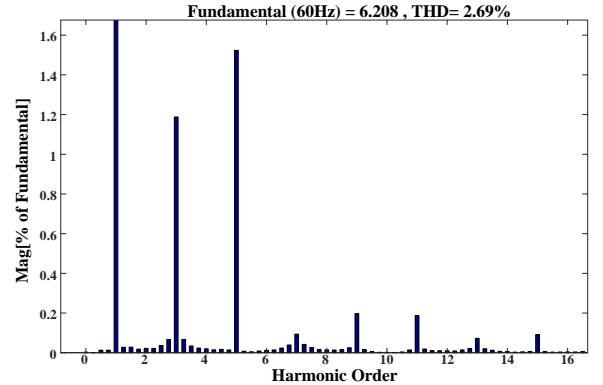


Fig. 8. FFT analysis in ac/dc PFC mode.

V. EXPERIMENT RESULTS

A 500W rated bidirectional ac/dc converter prototype is designed and tested. Parameters are summarized in Table I.

TABLE I
PARAMETERS OF THE PROTOTYPE

Name	Value
$S_1 \sim S_6$	C3D10060A
L_a, L_b, L_c	0.7mH
dc-link capacitor C	1mF
f_s	50kHz
AC side voltage	220Vrms, 60Hz
Controller	DSPACE MicroLabBox

Fig. 9 provides the picture of the experimental setup. In PFC mode, the waveforms are captured in Fig. 10. It can be seen that the input voltage and the input current are in phase. The current waveform is a sinusoidal wave. It can be seen that the input current is in phase with the input voltage. The output voltage is about 400V, the output power is 500W, and the corresponding power factor is 0.98. In this case, the boost ratio is relatively low. According to the circuit characteristics of PFC, when the boost ratio is low, its PF will be relatively low due to the high amplitude ripple current, so the power factor of 0.98 is acceptable.

The proposed converter can realize bidirectional energy flow. The feasibility of the PFC function in the charging process has been verified. When SPDT is in position 2, the battery pack can deliver ac power to an external load. The converter functions as an inverter. In our experiment, a resistive load is adopted. The entire system is equivalent to an inverter operating in island mode. To verify the feasibility of the circuit, the grid voltage was collected and used as a reference signal. The realization of the inverter is to regulate the power by controlling the phase relationship between current and grid voltage. Fig. 11 shows the ac current, ac voltage, and gate signal of switch S_3 . In this case, the battery voltage is 400 V, the ac voltage is 220 Vrms, and the output power is 500 W. Due to the resistive load, the ac current and voltage are in phase. As indicated by the experimental results, the output current is a standard sinusoidal waveform. The phase difference between the grid voltage and current is 180 degrees, which is equivalent to the grid obtaining energy from the battery. This shows that the system can realize V2G function.

The motor characteristics have a great influence on the converter performance. Since the windings of the motor are used as inductors, f_s directly affects the operating characteristics of the motor. To further explore the influence of f_s on system performance, the designed prototype is tested with different f_s . Fig. 12 shows the relationship between power factors and different switching frequencies. A higher f_s helps to achieve a better sinusoidal averaged input current. By increasing f_s , the power factor can be effectively improved.

In this work, motor windings are used as inductors. With high f_s , the eddy currents in both windings and core are large, which conflicts with the improvement of efficiency. Moreover, the inductor may change with the operating point of the motor due to hysteresis permeability. The solution is to use high-performance motors. However, in our experiment, the used motor performance is not superior. This puts an upper bound to f_s . Hence, the experimental power factor is not very ideal.

Another reason for non-ideal power factor is the zero-crossing distortion of the input current. According to the experimental waveform, it can be found that the input current has a plateau at the zero-crossing point. There are many spikes in the current waveform, inducing high-order harmonic components. This jeopardizes the THD of the input current and reducing the power factor.

Fig. 13 shows experimentally measured efficiency with the change of f_s . It can be found that the efficiency gradually increases as f_s increases. In normal cases, increasing f_s will reduce the current ripple, thereby reducing the conduction loss. Moreover, high f_s corresponds to a high power factor, which means fewer harmonic components. Therefore, the circulating current in the circuit will be very small, and the resulting

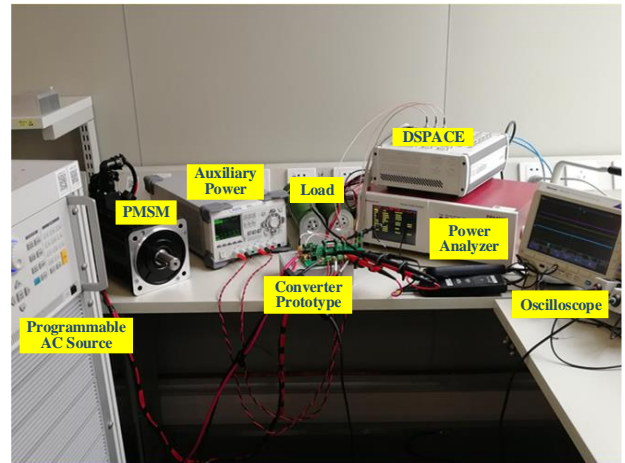


Fig. 9. Picture of the experimental setup.

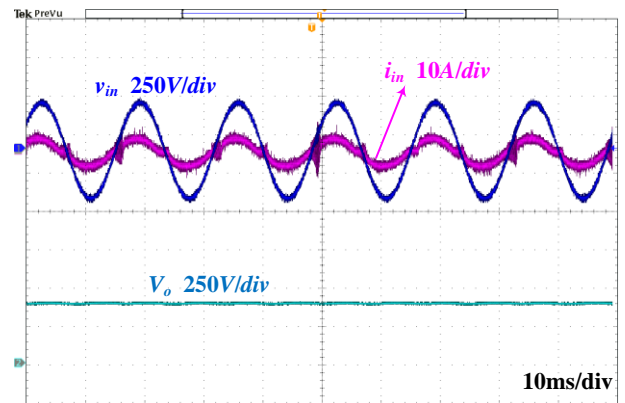


Fig. 10. Experimental waveforms in ac/dc PFC mode.

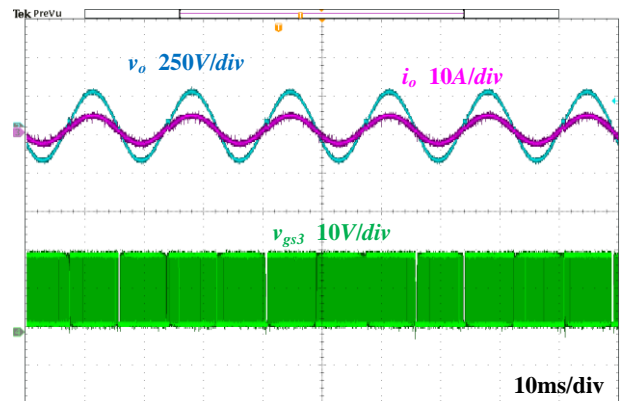


Fig. 11. Experimental waveforms in dc/ac inverter mode.

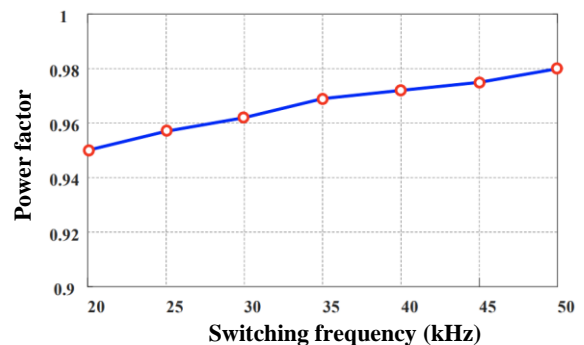


Fig. 12. Relationship between power factor and different f_s .

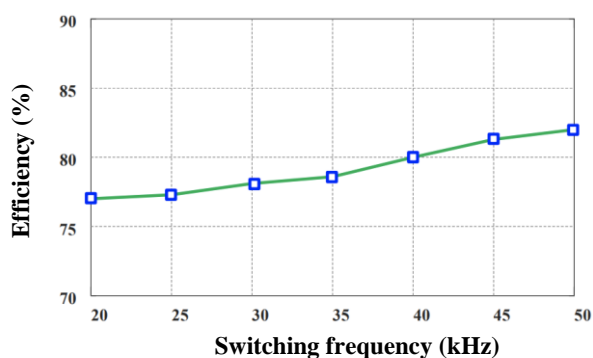


Fig. 13. Efficiency with different f_s .

conduction loss will be very low. In summary, as f_s increases, the gradual increase in efficiency is in line with objective facts. This also shows that a high power factor close to unity is always desired.

VI. CONCLUSION

In this work, a bidirectional ac/dc converter is proposed for PEV charging applications. The ac/dc converter is realized mainly using the motor drive and motor windings and is featured with an extremely high degree of integration. Reduced input current ripple is achieved due to the interleaving. Circuit analysis and control strategy are detailed.

A 500W bidirectional ac/dc converter prototype is designed, simulated, and tested to validate the concept. The experimental results show that the proposed converter can achieve 0.98 maximum power factor. The peak efficiency is 82%.

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