Optimal Design of H5 Bridge Based *LLC* Converter with Ultra-Wide Input Voltage Range and Synchronous Rectification

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***Abstract*—The dilemma between wide input range and narrow frequency band is a classic problem for the frequency modulated *LLC* converters. Using reconfiguring bridge can mitigate this issue effectively. However, there is a lack of systematic consideration in converter design and optimization. To address this challenge, this work introduces a six-mode *LLC* converter based on a reconfigurable H5 bridge, and systematically presents its optimal design methodology in ultra-wide input range applications. The dual *LLC* resonant tanks are driven by identical switching frequency, and provide a normalized gain range from 1 to 5. Synchronized rectification is employed on the secondary side to improve the gain and efficiency. The load distributions between dual tanks are analyzed in detail. It indicates that the equivalent output capacitance of the primary-side MOSFETs is reduced. This enhances the ZVS performance and reduces the circulating loss. The optimal design of transformer ensures a continuous voltage gain over adjacent modes. A 48V, 500W laboratory prototype is designed to validate the concept. The designed prototype is adapted to an 80V∼400V input range. The maximum efficiency is 96.95%.**

***Index Terms*—High step-down, *LLC* resonant converter, reconfigurable bridge, ultra-wide input range.**

I. Introduction

The *LLC* converter is widely used as isolated dc/dc converter due to its wide load range ZVS and high power density [1]–[3]. In energy storage unit powered electronic systems with low supply voltage, *LLC* converter needs to be adapted to an ultra-wide input voltage range and a high step-down ratio. In some systems, the energy storage unit acts as buffer. Thus, the nominal output voltage is in the middle of output voltage range [4]. Traditional *LLC* converter can not provide a good overall performance. For those applications, the frequency of *LLC* converter needs to swing over a wide range. This leads to increased conduction loss due to circulating current at low switching frequency. Conventionally, to squeeze the frequency band, a small magnetizing inductance is necessary [3], [5]. This results in a high magnetizing current, which leads to a large peak flux and the usage of high power-rating devices. In general, a narrow frequency band and moderate magnetizing inductance are expected in designing the ultra-wide input range *LLC* converters.

To achieve the target of wide input voltage range, many researches have been done. Some focus on developing *LLC* derived topologies. In [6], [7], an input-series-output-parallel converter is proposed. However, the number of control units scales up with the number of modules. This incurs a high control complexity. In [8], a two-stage *LLC*-buck topology is proposed. ZVS is realized in the buck stage at high input voltage. Nevertheless, with the decrease of input voltage, the ZVS of buck stage tends to get lost.

Another way to widen the input voltage range is using multi-mode converters. In [9], a reconfigurable *LLC* converter with dual bridges is proposed. It uses six MOSFETs to provide two bridge modes. It comes with high cost and low reliability. In [10], an *LLC* topology with two transformers and four modes is proposed. However, this technique is unsuitable for high step-down usages. When both transformers are enabled, the auxiliary MOSFETs suffer from high voltage stresses. In [11], we propose a modified four-mode gain *LLC* converter using a reconfigurable H5 bridge. Furthermore, in [12], the four-mode gain is extended into a six-mode gain profile by introducing an asymmetric resonant tank. However, they are targeted for wide output range applications and there is a lack of systematic analysis.

This work extended the H5 bridge based *LLC* topology into ultra wide input range applications. Synchronized rectification is enforced to improve the efficiency performance under low voltage and high current. The schematic of the proposed converter is plotted in Fig. 1. To tolerant the mismatch between dual tanks, series capacitors are added to the secondary side of dual tanks. Analysis and modeling of H5 topology are illustrated. Load distribution between dual tanks is analyzed. Optimal design methodology for transformers to evenly cover the voltage range is shown.

II. Mode configuration

The converter uses a re-configurable bridge to achieve wide gain range. It has six operation modes. Each mode can works independently at its designed region. The detailed switch patterns are shown in Fig. 2.

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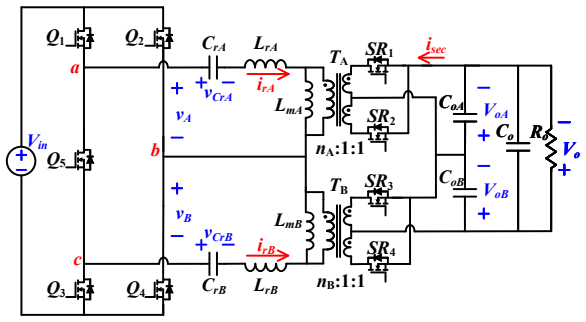


Fig. 1. Schematic of the H5 bridge based *LLC* converter.

In Mode 1, the inverter stage works as half bridge (HB) for resonant tank A (RT_A) and idle state for resonant tank B (RT_B). In Mode 2, the inverter stage works as HB for RT_B and idle state for RT_A. In Mode 3, the inverter stage works as HB for both RT_A and RT_B. In Mode 4, the inverter stage works as HB for RT_B and full bridge (FB) for RT_A. In Mode 5, the inverter stage works as HB for RT_A and FB for RT_B. In Mode 6, the inverter stage works as FB for both RT_A and RT_B.

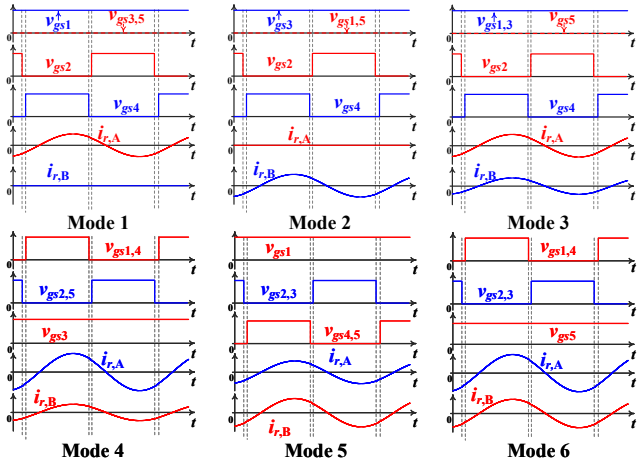


Fig. 2. Key steady state waveforms in different modes.

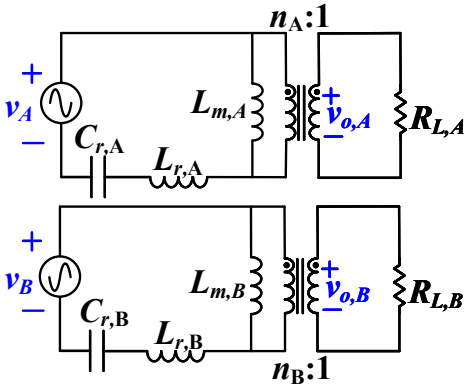


Fig. 3. Two resonant tanks model.

TABLE I
SUMMARY OF MODE CONFIGURATIONS

Mode Configuration	Resonant Tank Input			
	Description		V_A	V_B
I	HB for RT_A	idle for RT_B	$2V_{in}/\pi$	0
II	idle for RT_A	HB for RT_B	0	$2V_{in}/\pi$
III	HB for RT_A	HB for RT_B	$2V_{in}/\pi$	$2V_{in}/\pi$
IV	FB for RT_A	HB for RT_B	$4V_{in}/\pi$	$2V_{in}/\pi$
V	HB for RT_A	FB for RT_B	$2V_{in}/\pi$	$4V_{in}/\pi$
VI	FB for RT_A	FB forRT_B	$4V_{in}/\pi$	$4V_{in}/\pi$

III. Frequency-domain analysis of reconfigurable H5 bridge based resonant converter

A. Load distribution between dual tanks of H5 topology

For the H5 topology in Fig. 1, it can be divided into two sub-circuits following the voltage division principle as shown in Fig. 3, where v_A and v_B are two fundamental components of v_{ab} and v_{cb}. v_A and v_B have completely opposite phases. V_A and V_B are their amplitudes, respectively, as summarized in TABLE I.

According to the principle of voltage division,

$$R_{L,A} + R_{L,B} = R_o. \tag{1}$$

Then, the output power ratio is determined. I_{sec} is the root mean square (RMS) of output current.

$$\frac{P_{o,A}}{P_{o,B}} = \frac{I_{sec}^2 R_{L,A}}{I_{sec}^2 R_{L,B}} = \frac{V_{o,A}}{V_{o,B}} = \frac{n_B V_A G_A}{n_A V_B G_B} \tag{2}$$

G_A and G_B are transfer functions of two resonant tanks.

$$\begin{aligned} G_i|_{i=A,B} &= n_i V_{o,i}/V_i \\ &= \frac{F_i^2 L_{n,i}}{\sqrt{(F_i^2(1+L_{n,i})-1)^2 + (F_i^2-1)^2 L_{n,i}^2 Q_i^2 F_i^2}} \end{aligned} \tag{3}$$

F_i is the normalized switching frequency. $L_{n,i}$ is the inductance ratio. Q_i is the figure of merit (FOM).

$$F_i = f_{s,i}/f_{r1,i} \tag{4}$$

$$L_{n,i} = L_{m,i}/L_{r,i} \tag{5}$$

$$Q_i = \pi^2 \left(\sqrt{L_{r,i}/C_{r,i}}\right)/(8n_i^2 R_{L,i}) \tag{6}$$

To make the output power distributed evenly between two resonant tanks, their gain range is better to have a similar growth rate. Due to Mode IV and Mode V mirror each other, series resonant frequencies of RT_A and RT_B are expected to match. Thus, the normalized switching frequencies of RT_A and RT_B can be treated as the same.

$$F_A \approx F_B \tag{7}$$

B. Iterative model for load distribution

From (2), at series resonant frequencies,

$$\frac{R_{L,A}}{R_{L,B}} = \frac{V_{o,A}}{V_{o,B}} = \frac{n_B V_A}{n_A V_B}. \tag{8}$$

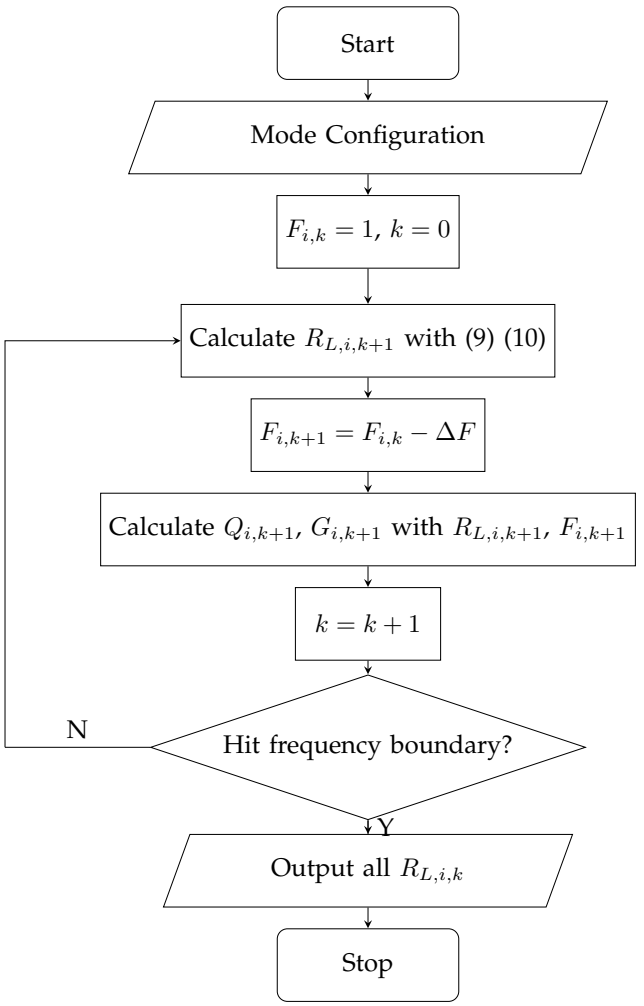


Fig. 4. Flow chat of the iterative model.

Since the secondary side is series connected, $R_{L,A}$ will change if $R_{L,B}$ varies. In a specific mode, load distribution does not demonstrate a discontinuity between adjacent frequencies.

$$R_{L,A,k+1}=\frac{n_B V_A G_{A,k}}{n_B V_A G_{A,k}+n_A V_B G_{B,k}}R_o \tag{9}$$

$$R_{L,B,k+1}=\frac{n_A V_B G_{B,k}}{n_B V_A G_{A,k}+n_A V_B G_{B,k}}R_o \tag{10}$$

To calculate the voltage gains at $F_{i,k+1}$, $R_{L,i,k+1}$ is used.

$$F_{i,k+1}=F_{i,k}-\Delta F \tag{11}$$

ΔF is the step of F_k.

When the switching frequency is below series resonant frequency, $\Delta F \geq 0$. When the switching frequency is above series resonant frequency, $\Delta F \leq 0$.

C. Input impedence and boundary gain

In Fig. 3, the input impedances of resonant tanks are

$$\begin{aligned}Z_{in,i}=&\frac{F_i^2 L_{n,i}^2 Q_i}{1+F_i^2 Q_i^2 L_{n,i}^2}\sqrt{\frac{L_{r,i}}{C_{r,i}}}\\&+j\frac{F_i L_{n,i}}{1+F_i^2 Q_i^2 L_{n,i}^2}\sqrt{\frac{L_{r,i}}{C_{r,i}}}+j\frac{F_i^2-1}{F_i}\sqrt{\frac{L_{r,i}}{C_{r,i}}}\end{aligned} \tag{12}$$

The peak gain occurs at resistive input impedance point. At that point, input impedance has no imaginary part.

$$\begin{aligned}\mathrm{Im}(Z_{in,i})=&\frac{F_{i,\min} L_{n,i}}{1+F_{i,\min}^2 Q_i^2 L_{n,i}^2}\sqrt{\frac{L_{r,i}}{C_{r,i}}}\\&+\frac{F_{i,\min}^2-1}{F_{i,\min}}\sqrt{\frac{L_{r,i}}{C_{r,i}}}=0\end{aligned} \tag{13}$$

At the peak gain point, the corresponding maximum FOM can be calculated.

$$Q_{i,\max}=\sqrt{\frac{1}{L_{n,i}-L_{n,i}F_{i,\min}^2}-\frac{1}{(L_{n,i}F_{i,\min})^2}} \tag{14}$$

From (3), design of the *LLC* converter should be able to achieve the maximum gain at heavy load and the minimum gain at light load.

$$\begin{aligned}G_{i,\max}&=G_i(F_{i,\min},Q_{i,\max})\\&=\frac{F_{i,\min}L_{n,i}}{\sqrt{F_{i,\min}^2(L_{n,i}^2+L_{n,i})-L_{n,i}}}\end{aligned} \tag{15}$$

$$\begin{aligned}G_{i,\min}&=\lim_{Q_i\to 0}G_i(F_{i,\max},Q_i)\\&=\frac{F_{i,\max}^2 L_{n,i}}{\left(F_{i,\max}^2(1+L_{n,i})-1\right)}\end{aligned} \tag{16}$$

IV. Gain range analysis

A. Evenly distributed mode configuration boundary

With six modes in H5 topology, the gain range can be widely expanded. Since the output voltage is regulated to be constant, the division of input voltage ranges needs to be optimized. At the resonant point,

$$\begin{cases}V_o/V_{in,M1}=\frac{1}{2}\frac{G_A}{n_A}=\frac{1}{2}\frac{1}{n_A}\\V_o/V_{in,M2}=\frac{1}{2}\frac{G_B}{n_B}=\frac{1}{2}\frac{1}{n_B}\\V_o/V_{in,M3}=\frac{1}{2}(\frac{G_A}{n_A}+\frac{G_B}{n_B})=\frac{1}{2}(\frac{1}{n_A}+\frac{1}{n_B})\\V_o/V_{in,M4}=\frac{G_A}{n_A}+\frac{1}{2}\frac{G_B}{n_B}=\frac{1}{n_A}+\frac{1}{2}\frac{1}{n_B}\\V_o/V_{in,M5}=\frac{1}{2}\frac{G_A}{n_A}+\frac{G_B}{n_B}=\frac{1}{2}\frac{1}{n_A}+\frac{1}{n_B}\\V_o/V_{in,M6}=\frac{G_A}{n_A}+\frac{G_B}{n_B}=\frac{1}{n_A}+\frac{1}{n_B}\end{cases} \tag{17}$$

It should be noted that n_B=*k* n_A, and $V_{in,Mi}$(*i* = 1,2,3,4,5,6) is distributed evenly.

$$\begin{aligned}u=&\left(V_{in,M1}-V_{in,M2}\right)^2+\left(V_{in,M2}-V_{in,M3}\right)^2\\&+\left(V_{in,M3}-V_{in,M4}\right)^2+\left(V_{in,M4}-V_{in,M5}\right)^2\\&+\left(V_{in,M5}-V_{in,M6}\right)^2\end{aligned} \tag{18}$$

The six modes are fully utilized with the minimum *u*. In this situation, *k*=3/4.

B. Continuous voltage gain range

Since in Mode 1, the H5 bridge is operated in half bridge mode, according to (3), (15) the maximum conversion ratio of Mode 1 is

$$M_{\max,1} = \frac{V_o}{V_{in,M1,\min}} = \frac{G_{\max,1,A}}{2n_A} \tag{19}$$

according to (16) the minimum conversion ratio of Mode 2 is

$$M_{\min,2} = \frac{V_o}{V_{in,M2,\max}} = \frac{G_{\min,2,B}}{2n_B} \tag{20}$$

Since the output voltage is constant V_o, $M_{\min,2}$should be larger than $M_{\max,1}$

$$M_{\min,2} \geq M_{\max,1} \tag{21}$$

Similarily, the maximum conversion ratios of other modes are:

$$M_{\max,2} = \frac{V_o}{V_{in,M2,\min}} = \frac{G_{\max,2,B}}{2n_B} \tag{22}$$

$$M_{\max,3} = \frac{V_o}{V_{in,M3,\min}} = \frac{G_{\max,3,A}}{2n_A} + \frac{G_{\max,3,B}}{2n_B} \tag{23}$$

$$M_{\max,4} = \frac{V_o}{V_{in,M4,\min}} = \frac{G_{\max,4,A}}{n_A} + \frac{G_{\max,4,B}}{2n_B} \tag{24}$$

$$M_{\max,5} = \frac{V_o}{V_{in,M5,\min}} = \frac{G_{\max,5,A}}{2n_A} + \frac{G_{\max,5,B}}{n_B} \tag{25}$$

$$M_{\max,6} = \frac{V_o}{V_{in,M6,\min}} = \frac{G_{\max,6,A}}{n_A} + \frac{G_{\max,6,B}}{n_B} \tag{26}$$

The minimum conversion ratio of other modes are:

$$M_{\min,1} = \frac{V_o}{V_{in,M1,\max}} = \frac{G_{\min,1,A}}{2n_A} \tag{27}$$

$$M_{\min,3} = \frac{V_o}{V_{in,M3,\max}} = \frac{G_{\min,3,A}}{2n_A} + \frac{G_{\min,3,B}}{2n_B} \tag{28}$$

$$M_{\min,4} = \frac{V_o}{V_{in,M4,\max}} = \frac{G_{\min,4,A}}{n_A} + \frac{G_{\min,4,B}}{2n_B} \tag{29}$$

$$M_{\min,5} = \frac{V_o}{V_{in,M5,\max}} = \frac{G_{\min,5,A}}{2n_A} + \frac{G_{\min,5,B}}{n_B} \tag{30}$$

$$M_{\min,6} = \frac{V_o}{V_{in,M6,\max}} = \frac{G_{\min,6,A}}{n_A} + \frac{G_{\min,6,B}}{n_B} \tag{31}$$

To achieve a continuous voltage gain range,

$$M_{\min,2} \geq M_{\max,1} \tag{32}$$

$$M_{\min,3} \geq M_{\max,2} \tag{33}$$

$$M_{\min,4} \geq M_{\max,3} \tag{34}$$

$$M_{\min,5} \geq M_{\max,4} \tag{35}$$

$$M_{\min,6} \geq M_{\max,5} \tag{36}$$

C. Parameter calculation

The relationship among quality factor, turns ratio, resonant capacitance, equivalent ac load and resonant frequency can be expressed as,

$$Q_i f_{r1,i} = \sqrt{\frac{L_{r,i}}{C_{r,i}}} \frac{1}{n_i^2 R_{L,i}} \frac{1}{2\pi\sqrt{L_{r,i}C_{r,i}}} = \frac{1}{2\pi n_i^2 C_{r,i} R_{L,i}} \tag{37}$$

Thus, resonant capacitance have a minimum value:

$$\begin{aligned} Q_i &= \frac{1}{2\pi n_i^2 C_{r,i} R_{L,i} f_{r,i}} \leq Q_{i,\max} \\ &\Rightarrow C_{r,i} \geq \frac{1}{2\pi n_i^2 Q_{i,\max} R_{L,i,\min} f_{r1,i}} \end{aligned} \tag{38}$$

With the minimum resonant capacitance, the maximum resonant inductance can be achieved,

$$L_{r,i} = \frac{1}{(2\pi f_{r1,i})^2 C_{r,i}} \tag{39}$$

With the designed inductance ratio , the magnetizing inductance can be calculated,

$$L_{m,i} = L_{n,i} L_{r,i} \tag{40}$$

L_m should provide enough energy to facilitate the ZVS,

$$\begin{aligned} &\frac{1}{2}(L_{r,A} + L_{m,A}) \left(\frac{n_A V_{o,A}}{L_{m,A}} \frac{T_s}{4}\right)^2 \\ &+ \frac{1}{2}(L_{r,B} + L_{m,B}) \left(\frac{n_B V_{o,B}}{L_{m,B}} \frac{T_s}{4}\right)^2 \geq \frac{1}{2} C_{eq} V_{in}^2 \end{aligned} \tag{41}$$

$$C_{eq} = 4C_{oss} + C_{stray} \tag{42}$$

C_{stray} is the stray capacitance due to PCB parasitics. The final $L_{m,A}$ and $L_{m,B}$ should satisfy requirements of both gain and ZVS.

V. Loss analysis

A. Conduction loss

Main part of conduction loss consists of two parts: semiconductor loss, copper loss and parasitic loss. Semiconductor loss is introduced by $R_{ds,on}$ of MOSFETs channel and V_d of body diodes. Copper loss is the loss on transmission line and inductor windings. Parasitic loss is introduced by equivalent series resistance of resonant capacitors, input and output capacitors. Parasitic loss can be reduced by parelling resonant capacitors and wide copper foils.

1) Semiconductor loss: Semiconductor loss is mainly determined by the peak of resonant current and secondary current [13].

$$I_{Lr,i,\text{peak}} = \frac{\sqrt{2}}{8} \frac{V_{o,i}}{n_i R_{L,i}} \sqrt{\frac{2n_i^4 R_{L,i}^2}{L_{m,i}^2 f_s^2} + 8\pi^2} \tag{43}$$

$$I_{\text{sec},i,\text{peak}} = \frac{\sqrt{2}}{4} \frac{V_{o,i}}{n_i R_{L,i}} \sqrt{\frac{5\pi^2 - 48}{12\pi^2} \frac{n_i^4 R_{L,i}^2}{L_{m,i}^2 f_s^2} + \pi^2} \tag{44}$$

So, a larger magnetizing inductance or a smaller MOSFET on resistance can reduce the semiconductor loss. A lower frequency makes a larger peak current. Thus, a wide frequency band will cause large loss.

2) Copper loss: Copper loss consists of two aspects. One is the PCB transimission line loss; another is the magnetizing component conduction loss.

PCB transimission line loss is mainly determined by the ac resistance of copper foils due to the skin effect. The skin depth ξ is determined in [14].

$$\xi = \frac{1}{\sqrt{\pi f_s \mu g}} \tag{45}$$

f_s is the switching frequency. μ is the absolute magnetic permeability of the conductor. g is the conductivity of the conductor in $\mathrm{S/m}$. If the copper foil is thinner than the skin depth, then the ac resistance's effect is mitigated.

The magnetic component conduction loss is due to the proximity effect of inductor or transformer windings. To inductors, for a M layer winding, since it can not have a interleave winding, the proximity effect makes an increased ac resistance [15].

$$R_{\mathrm{proxi}} = \frac{1}{3}\frac{h}{\xi}(2M^2+1)R_{dc} \tag{46}$$

h is the winding thickness. To a litz wire, $h/\xi \approx 1$

To some ferrite magnetic components with large air gaps, the fringing effect also needs to be considered. The accurate loss can be only determined by finite element simulations. A qualitative relation of this part of loss is determined by the physical winding turns and current amplitude. More windings, more loss. Larger current, larger loss. The physical winding turns is limited by the saturation of ferrite cores.

B. Switching loss

The converter works in ZVS region. Thus, the turn on loss of primary MOSFETs can be neglected. Total turn off loss of primary MOSFETs can be estimated [16].

$$P_{\mathrm{off}} = \frac{(I_{\mathrm{off}} t_{\mathrm{fall}})^2 f_s}{3C_{\mathrm{total}}} \tag{47}$$

From HB condition (Mode 1 and mode 2),

$$P_{\mathrm{off}} = \frac{(I_{\mathrm{off}} t_{\mathrm{fall}})^2 f_s}{6C_{\mathrm{oss}}} \tag{48}$$

From other condition (Mode 3-6),

$$P_{\mathrm{off}} = \frac{(I_{\mathrm{off}} t_{\mathrm{fall}})^2 f_s}{15C_{\mathrm{oss}}} \tag{49}$$

To secondary rectifiers, even when $f_s \geq f_r$ the rectifier current is in critical conduction mode (CRM). Due to the implementation of SR, ZVS for MOSFET is natural. Since main part of current is conducted in the channel of SR MOSFET, the reverse recovery of body diode is mitigated. The switching loss of secondary SR MOSFETs is very small.

C. Core loss

Core loss can be estimated with the Steinmetz equation [17].

$$p_{Lr,i} = C_m f^{\alpha} \hat{B}^{\beta}_{Lr,i} \tag{50}$$

$$p_{TX,i} = C_m f^{\alpha} \hat{B}^{\beta}_{TX,i} \tag{51}$$

For resonant inductors, since the resonant current has no dc bias, $\hat{B}_{Lr,A}$ and $\hat{B}_{Lr,B}$ is proportional to their corresponding peak resonant current.

For transformers, $\hat{B}_A$ and $\hat{B}_B$ are calculated as

$$\hat{B}_{TX,i} = \frac{\lambda_{p,i}}{2n_{s,i}A_e} = \frac{V_{o,i}}{4n_{s,i}A_e f_s} \tag{52}$$

$\lambda_{p,A}$ and $\lambda_{p,B}$ are the maximum volt-second on transformer. $n_{s,A}$ and $n_{s,B}$ are the secondary winding turns. A_e is the equivalent core areas.

When the converter works in mode 3 to 6, in primary side the conduction loss is reduced due to two parallel resonant tanks. Since the output voltage are divided into two parts, the core loss are reduced in mode 3 to 6. The converter can achieve a good efficiency at mode 3-6. When design the converter, the normal operating voltage should be designed there.

VI. Design considerations

A. Synchronized rectification

Researches have been done regarding sychronized rectification (SR) [18]–[21]. Their mechanisms can be divided into two catageroies: (a) signal launched (b) adapative control.

Signal launched SR is categorized into two types. Type one uses current sensor transformer and maintains good accuracy [22]. However, additional winding and core losses are introduced. Moreover, the magnetic components are bulky and difficult to design. Type two uses sensing v_{ds}, the voltage drop between the drain and source of SR MOSFETs [21], [23]. When v_{ds} is negative and reaches its body diode conducting threshold$V_{th,d}$, SR MOSFETs turn on; when v_{ds} is negative and reaches the turn off threshold$V_{th,c}$, which is manually set, SR MOSFETs turn off. When implementing this strategy, the PCB parasitic inductance might cause an early turn off of SR MOSFETs' channel. This incurs additional loss from body diodes. This strategy is very sensitive to noise and the accuracy is not moderate.

Adapative control in SR is widely used in digital control. In [20], the secondary MOSFETs are turned on synchronously with primary side. In the turning off process, a window counter to accumulate times of $v_{ds} < V_{th,d}$ is added to turn off the SR MOSFETs adapatively. It is easy to implement and successfully commercialized. Many commercial chips are made to implement the SR control. In this work, a SR commercial chip, SRK2001 by STMicroelectronics. is used to realize the SR.

B. Mode transition

In the mode transition process, one output voltage of two resonant tanks increases while the other decreases. In order to maintain a stable output voltage, the process should be done in a short period of time. As the primary side *LLC* is a current source [24], the secondary side delta connected rectifier capacitor can be charged quickly. In our work, the output inductance ratio is selected empirically **a)** to maintain a good output regulation, **b)** to achieve a smooth mode switching and **c)** to tolerate the unequal resonant current.

$$C_{oA} = C_{o,B} = \frac{1}{100} C_o \tag{53}$$

VII. Experimental Results

A. Design parameters

The input range of the designed prototype is set as 80V∼400V. The resonant frequency of two tanks are designed at 100kHz.

TABLE II
Design Parameters

Parameters	Value
$Q_1 - Q_5$	SCT 3120AL
$L_{m,A}(\mu H)$	182.3
$L_{r,A}(\mu H)$	38.2
$C_{r,A}(nF)$	64.9
$L_{m,B}(\mu H)$	147.64
$L_{r,B}(\mu H)$	30.5
$C_{r,B}(nF)$	84.5
n_A	16:4:4
n_B	15:5:5
$SR_1 - SR_4$	IRFB 4115
C_o (μF)	100
$C_{o,A}, C_{o,B}$ (μF)	1

B. ZVS verification

ZVS verification waveforms are shown in Fig. 5. As shown, the designed parameters facilitate a good ZVS performance in different operation modes.

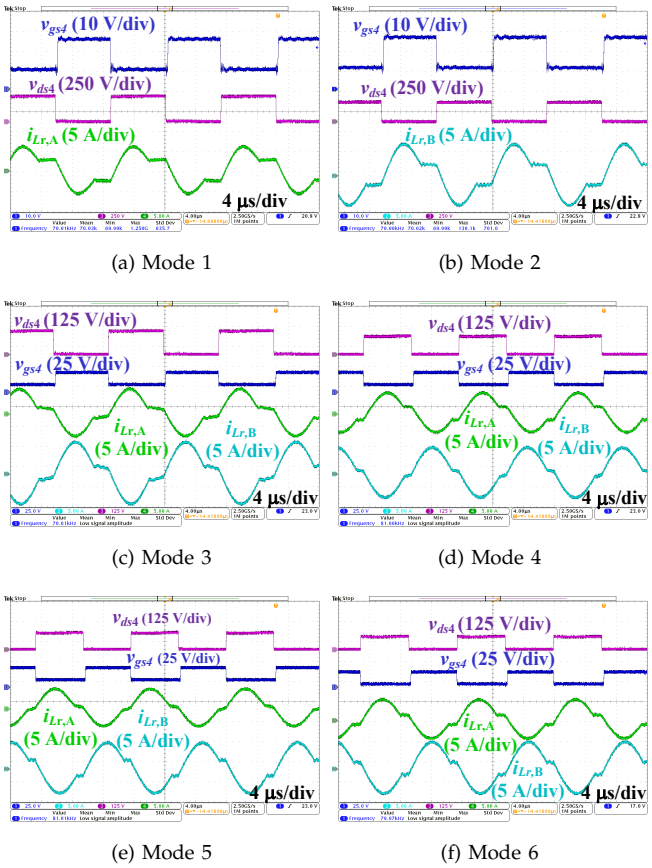
The steady-state experimental waveforms in Mode 3,4,5 and 6 are captured in Fig.6. From these figures, both RT_A and RT_B work well in HB or FB. All these waveforms are captured at 500W.

C. Synchronized rectification

The synchronized rectifier strategy uses commercial ICs. The experiment waveforms are shown in Fig. 7. From the result, the SR performance is good both in above resonance and below resonance situation.

D. Mode transition

Mode transition experiments are done in this work. Fig. 8 demonstrates the transients during the mode transitions. As shown, the transitions are smooth and the output voltage is stable.

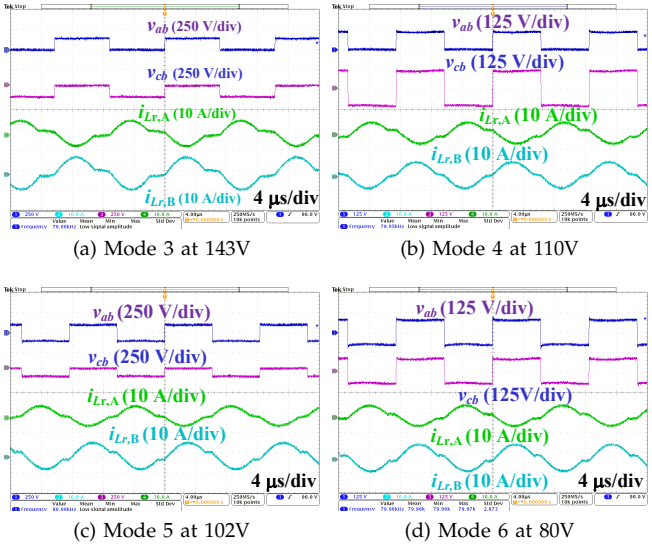


(a) Mode 1 (b) Mode 2

(c) Mode 3 (d) Mode 4

(e) Mode 5 (f) Mode 6

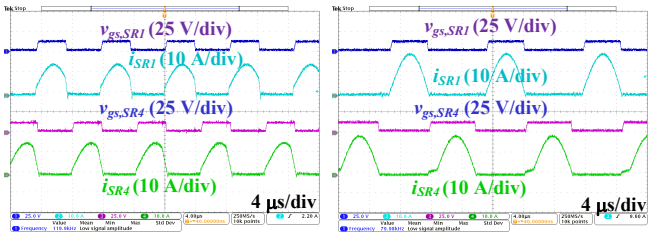
Fig. 5. ZVS verification in different modes.



(a) Mode 3 at 143V (b) Mode 4 at 110V

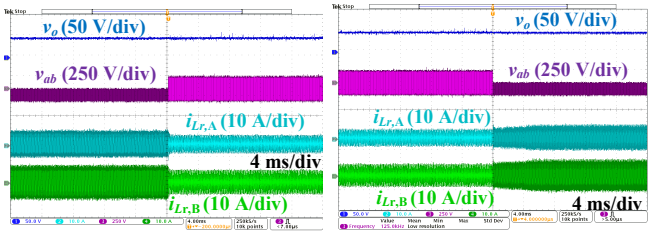
(c) Mode 5 at 102V (d) Mode 6 at 80V

Fig. 6. Working waveforms in Mode 3,4,5 and 6.

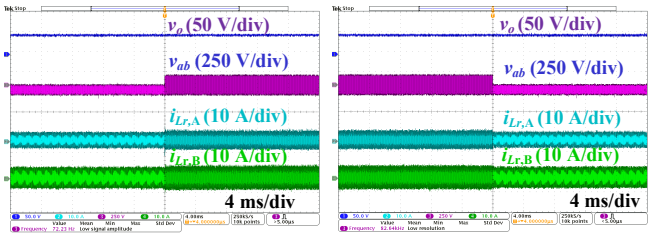


(a) Working above resonance (b) Working below resonance

Fig. 7. Synchronized rectifier waveforms at 500W output power.



(a) Switching from Mode 3 to Mode 4 at 150V 500W (b) Switching from Mode 4 to Mode 3 at 150V 500W



(c) Switching from Mode 4 to Mode 5 at 120V 500W (d) Switching from Mode 5 to Mode 4 at 120V 500W

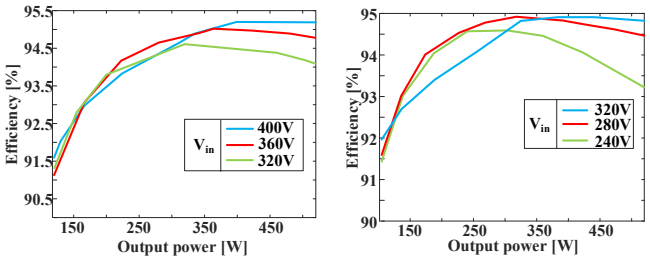
Fig. 8. Mode switching waveforms.

E. Efficiency

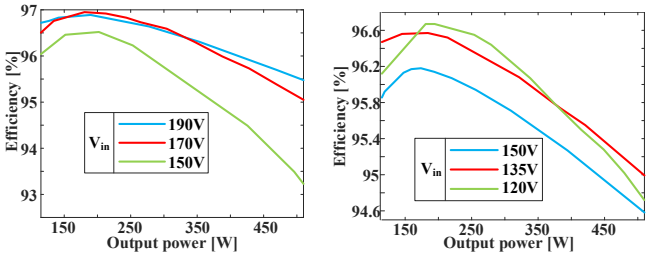
Conversion efficiency in six modes at different power levels are measured and plotted in Fig. 9. It can be observed that the converter working in mode 3-6 demonstrates a higher efficiency. In order to provide a smooth mode transient, the overlap zone between two modes are designed to avoid a frequent mode transition.

VIII. Conclusions

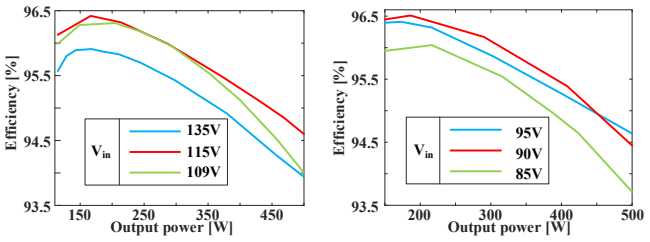
In this work, a six-mode dual tank resonant converter based on a re-configurable H5 bridge is proposed for high step-down applications. The optimal design method is detailed. An iterative gain model is presented to estimate the load distribution. A 500W prototype is designed to verify the model. It provides 5 times normalized peak gain. The input voltage range is fully covered. Losses component are estimated. The maximum efficiency is 96.95%. A wide ZVS range and smooth mode transitions are achieved experimentally.



(a) Mode 1 (b) Mode 2



(c) Mode 3 (d) Mode 4



(e) Mode 5 (f) Mode 6

Fig. 9. Efficiency in different modes.

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