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Design Methodology to Reduce the Lumped Winding Capacitance of Spiral Winding Transformer in LLC converters

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***Abstract*—In LLC converters, the transformer's lumped winding parasitic capacitance degrades the zero-voltage-switching performance as well as power delivery capability. However, the literature survey indicates that there is still a lack of a systematic methodology to guide the optimal winding of the transformer. In this paper, a method to reduce the parasitic capacitance is proposed. The mechanism of the parasitic lumped winding capacitance in spiral winding transformer is detailed. A performance comparison between the conventional winding and proposed winding is conducted experimentally. The experimental results show that using the proposed design, the lumped winding capacitance is reduced from 14.40pF/turn to 1.76pF/turn.**

***Index Terms*—Intra-winding capacitance, inter-winding capacitance, LLC, spiral winding transformer.**

I. Introduction

LLC converter is a prevalent isolated dc/dc topology. Fig. 1 shows the schematic of a classic half-bridge LLC converter. In the deadband, the magnetizing current charges the primary side MOSFET capacitance (C_{oss}), secondary side diode capacitance (C_d) and the lumped winding capacitance (C_{tr}). As illustrated in Fig. 2, the resonant capacitor (C_r) is neglected since $C_{oss} \ll C_r$. The C_{tr} and C_d induce a high-frequency oscillation [1] and lead to the regulation issue [1]–[3]. In the worst case, all magnetizing current is used to charge C_{tr} and C_d before the primary side reaches zero-voltage-switching (ZVS), which degrades the performance of ZVS. Moreover, the power delivery capability is reduced with a large C_{tr}, as shown in Fig. 3.

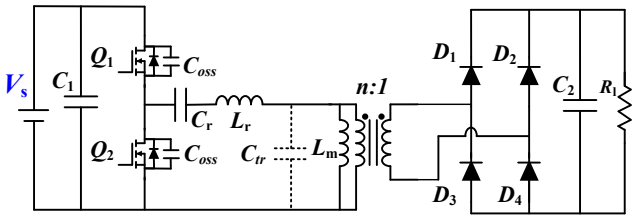

Fig. 1. Schematic of classic half bridge LLC converter.

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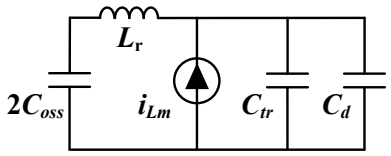

Fig. 2. Equivalent circuit of LLC converter in deadband.

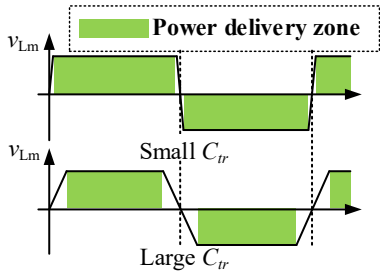

Fig. 3. Comparison of power delivery capability.

C_{tr} origins from two aspects as shown in Fig. 4. The capacitance between different windings is inter-winding capacitance (C_{inter}). The capacitance within the same windings is intra-winding capacitance (C_{intra}). C_{tr} in this paper considers the zero ac common-voltage cases, as demonstrated in Fig. 4(b).

Many research works have been conducted to analyze the parasitic capacitance of the transformer. In [4]–[7], the parasitic capacitance is calculated and measured via frequency sweep. The first-order parallel resonant frequency is induced

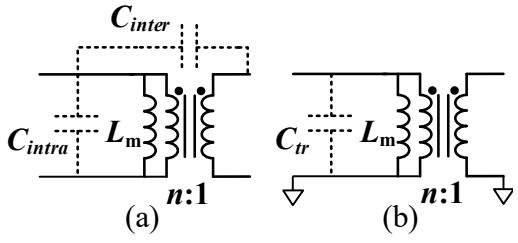

Fig. 4. Transformer (a) inter-winding capacitance and intra-winding capacitance; (b) Zero common voltage lumped capacitance C_{tr}.

by self-inductance and the lumped capacitance after setting the common-mode voltage between the primary side and secondary side.

Methods to reduce C_{intra} and C_{inter} have also been studied. In [1], authors suggest reducing C_{intra} by changing the dielectric material. In [3], C_{intra} is reduced by misaligning two adjacent layers. In [8], ground points are inserted in the layers to reduce C_{intra}.In [9], a shielding layer is added to reduce C_{inter}. In [10], the primary side and secondary side planes maintain a $180°$ difference to reduce C_{inter}. In [11] insulators are added so that the interleaved windings don't cause a rapid increase of C_{inter}. It should be noted that all these above-mentioned methods are modeled on planar magnetics.

However, for spiral windings, those arrangements cannot be as precisely controlled as what we can do on printed-circuit-board. The spiral winding structure is different from those in planar magnetics, where multi-layer and multi-windings are frequently used, leading to various conditions. Generally, more choices can be made for spiral winding connections than planar windings. Moreover, although the spiral winding transformers are classic, most of the winding capacitance literature focus on the planar magnetics. There lacks a methodology to guide the design of spiral winding transformers with low lumped winding capacitance.

In this work, the static spiral winding capacitance and lumped winding capacitance are modeled. Methods to reduce the static winding capacitance is analyzed. Both intra-winding capacitance and inter-winding capacitance are considered. Effect of the inter-winding capacitance on the lumped capacitance is investigated. An optimization methodology is proposed to reduce the lumped winding capacitance. The lumped winding capacitance is reduced from 14.40pF/turn to 1.76pF/turn.

The spiral winding capacitance modelling and analysis are in Section II. Section III is the proposed optimization methodology for reducing the lumped winding capacitance. The experimental verification is in Section IV. Conclusions are in Section V.

II. Capacitance Modelling in Spiral Windings

A. Static Winding Capacitance

In Fig. 5(a), spiral windings $a_0 \sim a_3$, $b_0 \sim b_3$ are evenly winded around the center leg in two layers. In Fig. 5(b), those eight windings are winded in an alternative way to fill the window area. For mechanical stability, only the winding structure that is symmetrical to the vertical direction is considered. The intersecting surface potentials are named after their surface names. R_1 is the radius of the bobbin on the core center leg. Since the distance between the core and windings are much greater than that among windings, the core-winding capacitance is ignored in the analysis.

The number of turns are extended into N turns with m layer and n windings per layer. $N = mn$. If $N = 1$, there is no overlapped area due to single winding. Hence, the lumped capacitance C_{lump} is zero. However, $N = 1$ is not practical due to the restriction of the maximum flux. Parasitic capacitance

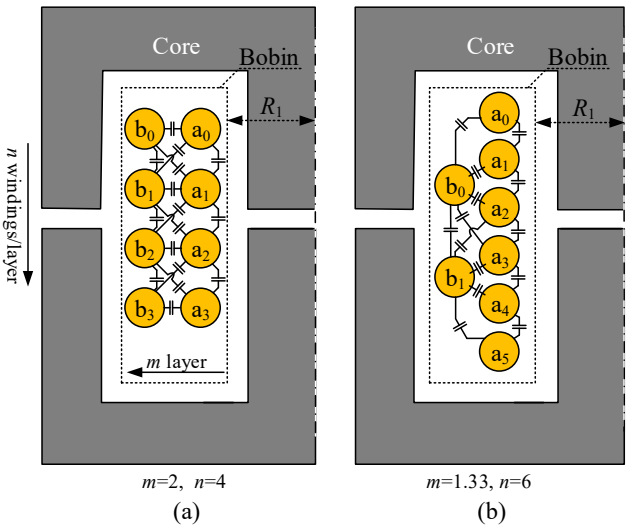

Fig. 5. (a) Spiral winding intersecting surface at $m = 2, n = 4$. (b) Spiral non-uniform windings at $m = 1.33, n = 6$.

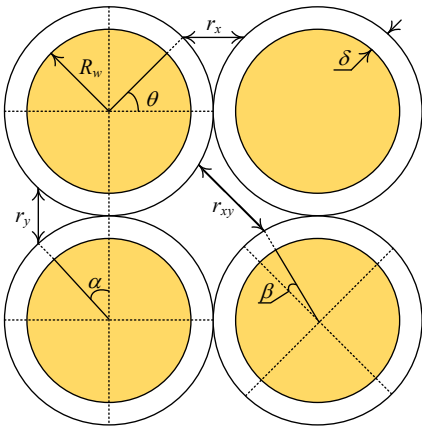

Fig. 6. Basic cell of spiral orthogonal windings.

exists between directly overlapped windings. Due to geometric symmetry, $C_{a_i b_{(i-1)}} = C_{a_{(i-1)} b_i} = C_{xy}$ are the diagonally capacitance. $C_{a_{(i-1)} b_{(i-1)}} = C_x$ are horizontal capacitance. $C_{a_{(i-1)} a_i} = C_{b_{(i-1)} b_i} = C_y$ are vertically capacitance.

To analyze C_x, C_y and C_{xy}, the basic cell of spiral orthogonal windings is illustrated in Fig. 6. δ is the insulated depth. R_w is the copper winding radius. The electric field inside the surface of the conductor is approximated to be zero. The horizontal capacitance consists of series connection of insulated capacitance $C_{x,i}$ and air-gap capacitance $C_{x,a}$. l_w is the mean turns length (MLT). Since $R_1 \gg R_w$, $l_w \approx 2\pi R_1$.

$$
\begin{aligned}
dC_{x,i} &= \epsilon_0 \epsilon_r \int_0^{l_w} dl \int_{R_w}^{R_w+\delta} \frac{r}{dr} d\theta = \frac{\epsilon_0 \epsilon_r l_w}{ln(\frac{R_w+\delta}{R_w})} d\theta, \\
dC_{x,a} &= \epsilon_0 \frac{l_w (R_w+\delta) d\theta}{r_x} \\
&= \epsilon_0 \frac{l_w (R_w+\delta)}{2(R_w+\delta)(1-cos(\theta))} d\theta, \\
dC_x &= \frac{2 dC_{x,i} dC_{x,a}}{2 dC_{x,i} + dC_{x,a}}.
\end{aligned}
\tag{1}
$$

The calculations of C_y and C_{xy} are similar due to geometric symmetry.

$$\begin{aligned} dC_{y,i} &= \frac{\epsilon_0 \epsilon_r l_w}{ln(\frac{R_w+\delta}{R_w})} d\alpha, \\ dC_{y,a} &= \epsilon_0 \frac{l_w}{2(1-cos(\alpha))} d\alpha, \\ dC_y &= \frac{2dC_{y,i}dC_{y,a}}{2dC_{y,i}+dC_{y,a}}, \end{aligned} \tag{2}$$

$$\begin{aligned} dC_{xy,i} &= \frac{\epsilon_0 \epsilon_r l_w}{ln(\frac{R_w+\delta}{R_w})} d\beta, \\ dC_{xy,a} &= \epsilon_0 \frac{l_w}{2(\sqrt{2}-cos(\alpha))} d\beta, \\ dC_{xy} &= \frac{2dC_{xy,i}dC_{xy,a}}{2dC_{xy,i}+dC_{xy,a}}. \end{aligned} \tag{3}$$

To get the total capacitance, do the integration,

$$\begin{aligned} C_x = \int_{-\pi/2}^{\pi/2} \frac{dC_x}{d\theta} d\theta,\ C_y = \int_{-\pi/2}^{\pi/2} \frac{dC_y}{d\alpha} d\alpha, \\ C_{xy} = \int_{-\pi/2}^{\pi/2} \frac{dC_{xy}}{d\beta} d\beta. \end{aligned} \tag{4}$$

According to (1),(2), and (3), the winding insulation capacitance under the same MLT is mainly determined by the ratio between δ and R_w. A thicker depth causes a lower capacitance with the same R_w. On the other hand, a smaller R_w can also reduce the capacitance with the same δ. The air-gap capacitance is only determined by the MLT. Hence, reducing the winding capacitance by decreasing the static capacitance can be achieved in two ways:

1) increase the insulation layer thickness;
2) decrease the winding length per turn, or MLT.

The first way is restricted by the magnetic core window utilizating rate. The insulating layer occupies the space of copper windings. The second way can be achieved with a small center leg radius core. However, it may increase the maximum flux and magnetic loss. Since the effect of the first way is inversely related to the distance, adding an insulation layer to fill the window area is simple and feasible without inducing additional loss.

B. Lumped Capacitance between Layers

The potential difference between 1) a_0 and a_1 is marked as U_{a0a1}; 2) a_0 and b_0 is noted as U_{a0b0}, and so on. All of them are determined by the winding connected sequence, e.g. the induced electromotive force. The winding capacitance has inner excitations between two adjacent nodes in Fig. 7(a), so the lumped capacitance is related to the winding connection sequence and can not be calculated as series or parallel connection type. In the lumped model in Fig. 7(b), the voltage on the whole windings is marked as U_{tot}.

In case as shown in Fig. 5(a), only these three directions of capacitive energy exists. Define the m^{th} layer has windings named as $k_0, k_1, ...k_n$; $(m-1)^{th}$ layer has windings named as $j_0, j_1, ...j_n$. In the following modelling, n is equal for each layer. Energy of capacitance between layer b_{i-1} and b_i is similar to that between layer a_{i-1} and a_i.

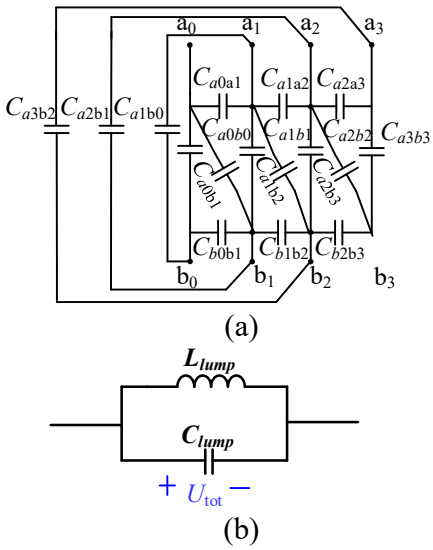

Fig. 7. Winding (a) circuit model with parasitics capacitance (b) lumped parasitic model

The horizontally overlapped area is much larger than the diagonally overlapped area. The diagonal capacitance has a longer distance between its overlapped area than those in horizontal and vertical capacitance. The vertically overlapped area is similar to the horizontally overlapped area. $C_{xy} < C_x \approx C_y$. However, the voltage across the diagonal direction may be very large. The energy stored in the diagonal capacitance can still be considerable in spiral windings. This property is different from the planar conditions. In planar conditions, the diagonal capacitance has nearly zero overlapped area if the winding width is the same due to rectangular winding shape. The capacitive energy stored in layers is shown in (5).

$$\begin{aligned} E_{a_{(i-1)}a_i} &= \frac{1}{2} U^2_{a_{(i-1)}a_i} C_{a_{(i-1)}a_i}, \\ E_{b_{(i-1)}a_i} &= \frac{1}{2} U^2_{b_{(i-1)}a_i} C_{a_i b_{(i-1)}}, \\ E_{a_{(i-1)}b_i} &= \frac{1}{2} U^2_{a_{(i-1)}b_i} C_{a_{(i-1)}b_i}, \\ E_{b_{(i-1)}a_{(i-1)}} &= \frac{1}{2} U^2_{b_{(i-1)}a_{(i-1)}} C_{a_{(i-1)}b_{(i-1)}}. \end{aligned} \tag{5}$$

The lumped capacitor model and the total energy E_{tot} can be calculated as (6).

ΔE_m is the energy increasement from layer j to layer k. It consists of three parts. The first part is the vertical capacitance energy incrementation. Specially, if $n = 1$, $C_y = 0$. The second part is the horizontal capacitance energy incrementation. The third part is the diagonal capacitance energy incrementation.

For non-uniform spiral windings as Fig. 5(b), the winding capacitance is more complicated. (m, n) in this condition is not an integer pair. In Fig. 5(a), due to the shielding effect of adjacent windings, the dominant winding capacitance consists of three directions. However, in Fig. 5(b) type, the winding b_0 has overlapped area with all windings near it, e.g. $a_0 - a_3$. Therefore, more parasitic capacitance appears and the total

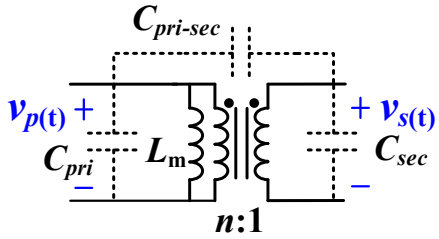

Fig. 8. Two windings transformer with three lumped capacitance in zero common mode voltage.

capacitive energy will be larger than situations where m and n are integers, e.g. Fig. 5(a).

$$
\begin{aligned}
E_{tot} &= \frac{1}{2}U_{tot}^2 C_{lump},\\
E_{tot} &= E_1 + \Delta E_2 + ... + \Delta E_m,\\
E_1 &= \frac{1}{2}C_y \sum_{i=1}^{n-1} U_{a_{(i-1)}a_i}^2,\\
\Delta E_2 =& \frac{1}{2}C_y \sum_{i=1}^{n-1} U_{b_{(i-1)}b_i}^2 + \frac{1}{2}C_x \sum_{i=1}^{n-1} U_{a_{(i-1)}b_{(i-1)}}^2\\
&+ \frac{1}{2}C_{xy} \sum_{i=1}^{n-1} (U_{a_i b_{(i-1)}}^2 + U_{a_{(i-1)}b_i}^2)\\
\Delta E_3 =& \frac{1}{2}C_y \sum_{i=1}^{n-1} U_{c_{(i-1)}c_i}^2 + \frac{1}{2}C_x \sum_{i=1}^{n-1} U_{b_{(i-1)}c_{(i-1)}}^2\\
&+ \frac{1}{2}C_{xy} \sum_{i=1}^{n-1} (U_{b_i c_{(i-1)}}^2 + U_{b_{(i-1)}c_i}^2),\ ...\\
\Delta E_m =& \frac{1}{2}C_y \sum_{i=1}^{n-1} U_{k_{(i-1)}k_i}^2 + \frac{1}{2}C_x \sum_{i=1}^{n-1} U_{j_{(i-1)}k_{(i-1)}}^2\\
&+ \frac{1}{2}C_{xy} \sum_{i=1}^{n-1} (U_{j_i k_{(i-1)}}^2 + U_{j_{(i-1)}k_i}^2).
\end{aligned}
\tag{6}
$$

C. The Transformer Capacitance Model

Fig. 8 shows the three lumped capacitance model for a two windings transformer. The primary side has intra-winding capacitance named after C_{pri}. The secondary side has intra-winding capacitance named after C_{sec}. C_{inter} between the primary and the secondary side is named after $C_{pri-sec}$. All those three capacitance can be calculated with (6). Moreover, from (6) the lumped transformer capacitance is independent from U_{tot}. To get the overall lumped capacitance, the inter-winding capacitance need to be transformed across a single port. Without loss of generality, the inter-winding capacitance is reflected to the primary side as $C_{ps,p}$. $\mathcal{L}\{v_s(t)\} = V_s,\ \mathcal{L}\{v_p(t)\} = V_p,\ \mathcal{L}\{i_p(t)\} = I_p$. In situations where the transformer is secondary side open circuit, it has equations as follows.

$$
\begin{aligned}
V_s &= \frac{1}{n}V_p,\\
I_p &= j\omega C_{pri-sec}(V_s - V_p),\\
j\omega C_{ps,p} &= \frac{V_s}{V_p} = \frac{n-1}{n} j\omega C_{pri-sec},\\
C_{tr} &= C_{pri} + C_{ps,p} + \frac{1}{n^2}C_{sec}.
\end{aligned}
\tag{7}
$$

Therefore, if the transformer turns ratio is $n = 1$, C_{inter} has no effects on C_{tr}. A higher n will has a larger effect from C_{inter} on the C_{tr}.

D. High Frequency Effects

1) Skin effect and Litz-wire equivalence: To analyze the parasitic capacitance, skin effect and proximity effect are ignored in above analysis for simplification. If considered, the current will distribute near the conductor surface. The electric field in the copper wire is not zero and complicated to calculate due to the Eddy current. Additional capacitive energy excited by skin effect becomes obvious. This leads to an increasement of the parasitic capacitance C_{tr}.

To mitigate this effect, Litz wire is always used. κ is the copper filling factor of Litz wire. Inside the Litz wire, circulating current is limited and electric field between strands inside a Litz wire is close to zero. Hence, the Litz wire with n strands radius r_w can be equivalently modelled as a solid wire with $R_{eq,w}$.

$$
\frac{n\pi r_w^2}{\kappa} = \pi R_{eq,w}^2. \tag{8}
$$

2) Proximity effect: The proximity effect doesn't affect the capacitance directly. However, to mitigate its effect, windings are always interleaved. Interleaved windings may increase the overlap area of inter-windings but decrease the overlap area of intra-windings. This leads to an increase in inter-winding capacitance and a reduction in intra-winding capacitance. For the transformer whose turns ratio is not unity, e.g. $n \neq 1$, the inter-windings capacitance also affect the total transformer C_{tr}.

III. Proposed Methodology to Reduce the Lumped Capacitance

For a N turns winding, design with low capacitive energy is that layer number m and winding number per turn n are both integers. Hence, the first step is to determine a N that equals the product of two integers. $N = mn$.

$$
\begin{aligned}
U_{a_{(i-1)}a_i} = U_{a_{(p-1)}a_p},\ U_{b_{(i-1)}b_i} = U_{b_{(p-1)}b_p},\\
U_{a_{(i-1)}b_{(i-1)}} = U_{a_{(p-1)}b_{(p-1)}},\ U_{a_i b_{(i-1)}} = U_{a_p b_{(p-1)}},\\
U_{c_{(i-1)}c_i} = U_{c_{(p-1)}c_p},\ U_{b_{(i-1)}c_{(i-1)}} = U_{b_{(p-1)}c_{(p-1)}},\\
U_{b_i c_{(i-1)}} = U_{b_p c_{(p-1)}},\ ...\ , U_{k_{(i-1)}k_i} = U_{k_{(p-1)}k_p},\\
U_{j_{(i-1)}k_{(i-1)}} = U_{j_{(p-1)}k_{(p-1)}},\ U_{j_i k_{(i-1)}} = U_{j_p k_{(p-1)}},\\
i = 1, 2, ..., n-1, p = 1, 2, ..., n-1.
\end{aligned}
\tag{9}
$$

In Fig.10, integer n is first chosen then m is determined. The energy of windings can be sorted into three categories:

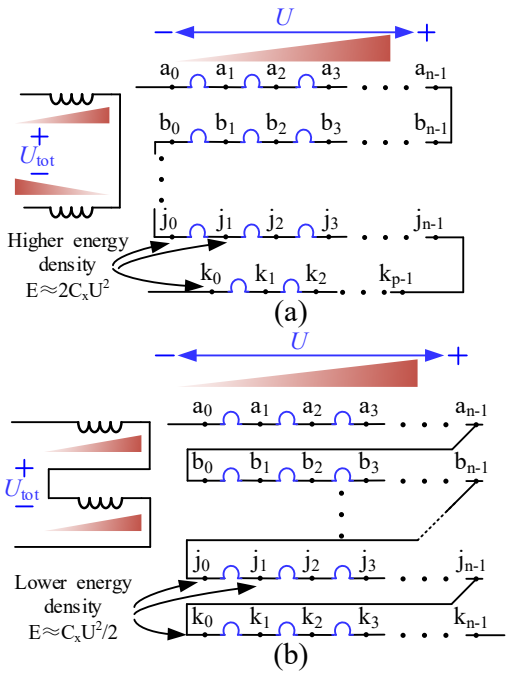

Fig. 9. (a) Conventional non-uniform connection sequence (b) uniform winding number connection.

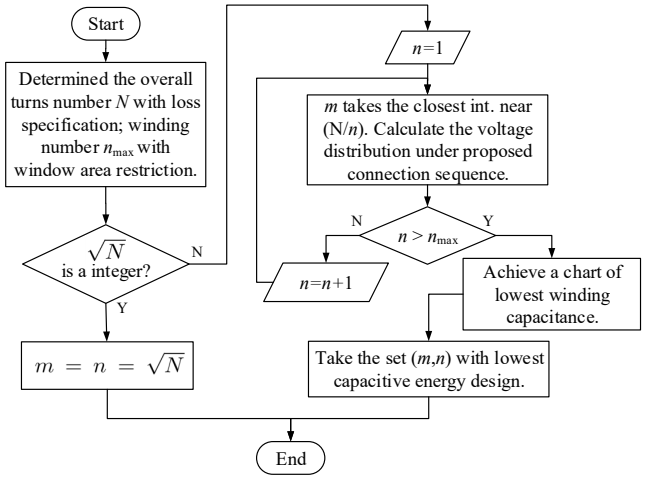

Fig. 10. Flow chart of the proposed methodology to reduce the winding capacitance.

a) Horizontal mutual capacitance energy related with C_x.
b) Diagonal mutual capacitance energy related to C_{xy}.
c) Vertical mutual capacitance energy related to C_y.
Therefore, the minimum horizontal capacitive energy happens when horizontal potential differences between two adjacent windings are equal. So do the vertical and diagonal direction capacitive energy, which is described in (9).

The potential difference distribution should satisfy the Kirchhoff's voltage law and Lenz's law. The studided case has zero ac common voltage as illustrated in Fig. 4, therefore the inter-winding capacitance can be optimized as well. Conventional method, as shown in Fig. 9(a) may fill the window height and leave some windings to another layer, e.g. $p \neq n$. Besides, it connects the adjacent windings to achieve a small winding resistance. However, in the perspective of winding capacitance, such a connection exhibits the worst energy distribution. Moreover, the non-uniform windings increase the overall capacitive energy. Connection demonstrated in Fig. 9(b) has a low winding energy. Since N is always a settled value with optimization of magnetic core loss and copper loss, $m = n = \sqrt{N}$ is the optimal lumped capacitance design if N is a square number.

However, such a situation is not always feasible. The proposed method is to minimize the total energy in the windings.

The design flow chart is shown in Fig. 10. The first step is to determine the overall turns number N. N is restricted to the maximum magnetic core loss:

$$B_{max} = \frac{V_T T_s}{4 N A_e}, \qquad P_{core,max} \geq V_c k_c f_s^{\alpha} B_{max}^{\beta}. \tag{10}$$

V_T is the tarnsformer terminal voltage on the N turns winding, n_s is the secondary winding number. A_e is the equivalent flux surface area. T_s is the switching period. k_c, α, β are coefficients determined by the core materials. V_c is the selected core volume. For secondary winding, $V_T = V_{RL}$. For primary winding, $V_T = V_s$ when the converter is working at the resonant point. If N is not a square number, calculate the voltage distribution in uniform connection from $n = 1$ to $n = n_{max}$. n_{max} is restricted by the window height. After that, we can achieve a chart of the optimal winding capacitance in each n case with (4)∼(9). Take the lowest one, then the accessible lowest capacitance design can be found.

IV. Experimental Results

To demonstrate a significant improvement compared with the conventional method, two interleaved LLC transformers are designed. The conventional design exhibits less overlapped area than the proposed method. The LLC converter is a 36V/20V design at 56 kHz resonant frequency. Note that the conventional way doesn't require the turns number to be a square number, so the counterpart transformer with the conventional method is designed with the minimum turns number.

The simulation results of Finite element analysis (FEA) is shown in Figs. 11 and 12. In the simulation, the common-mode voltage between the dot terminals is 10 V. The electric field distribution using the proposed design methodology is more evenly distributed than that in conventional types.

The frequency characteristics are compared in Figs. 13 and 14. The proposed methodology can achieve 2.24 times higher self-resonance frequency, from 530.884kHz to 1.318MHz with more turns compared with the conventional method.

The parameters comparison is listed in Tab. I. The first order self-resonance frequency is caused by C_{tr} and L_m. The proposed method reduces the winding capacitance significantly from 345.67pF to 63.40pF, or 14.40pF/turn to 1.76pF/turn. Therefore, the proposed method can achieve a smaller lumped capacitance with a larger winding turn number. The maximum

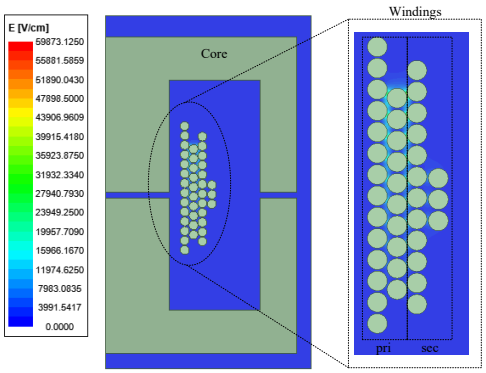

Fig. 11. Electrostatic FEA simulation using conventional non-uniform connection.

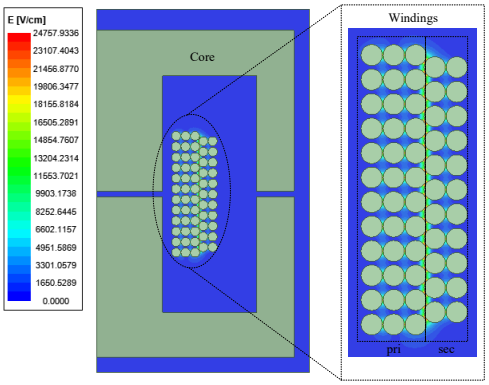

Fig. 12. Electrostatic FEA simulation using the proposed design methodology.

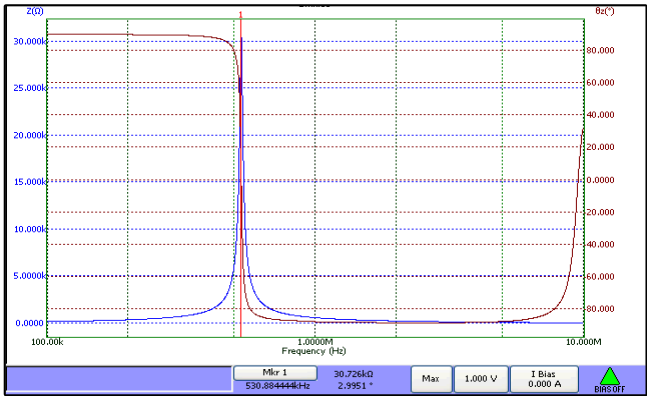

Fig. 13. Frequency sweep results of the transformer using conventional non-uniform connection.

TABLE I
TRANSFORMER PARAMETER COMPARISON

Transformer	Turns number	Magnetizing inductance L_m	Lumped winding capacitance C_{tr}
Conventional	(24):(15)	$L_{m,\text{conv}} = 260\text{uH}$	$C_{\text{conv}} = 345.67\text{pF}$
Proposed	(36):(22)	$L_{m,\text{pro}} = 230\text{uH}$	$C_{\text{pro}} = 63.40\text{pF}$

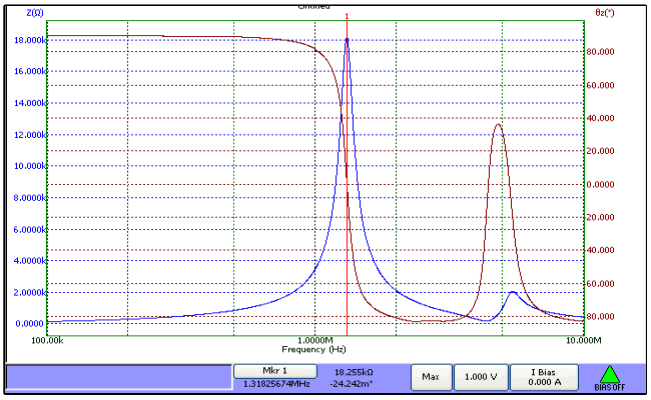

Fig. 14. Frequency sweep results of the transformer using the proposed design methodology.

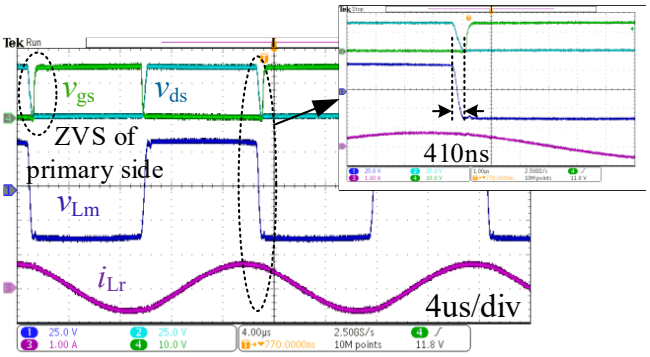

Fig. 15. Transformer voltage commutation time of conventional method.

flux can be reduced while the self-resonance frequency doesn't decrease. Less magnetic core loss and lower lumped winding capacitance can be achieved using the proposed optimization methodology.

The performance improvement in ZVS performance is compared in Figs. 15 and 16 at 20V, 0.4A output. The charging period of C_{tr} together with C_d and C_{oss} is reduced with the proposed methodology from $t_{\text{conv,m}} = 410ns$ to $t_{\text{pro,m}} = 300ns$. Time equivalent capacitance of the tested diode (C3D10060A) and MOSFET (IPW60R180P7) at 30V

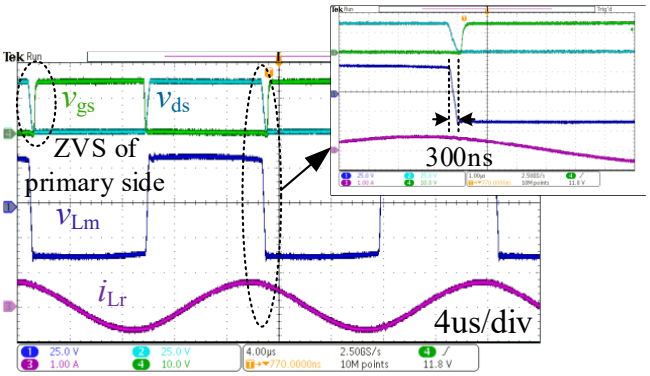

Fig. 16. Transformer voltage commutation time of proposed method.

from their datasheets is $C_d + 2C_{oss} = 1.25nF$. From Tab. I, the capacitance reduces

$$\frac{C_{\rm pro} + C_d + 2C_{oss}}{C_{\rm conv} + C_d + 2C_{oss}} = 82.3\%. \tag{11}$$

Consider the mismatch of the charging current i_{Lm}, the charging times have relationship as follows.

$$\frac{t_{\rm pro}}{\rm t_{conv}} = \frac{C_{\rm pro} + C_d + 2C_{oss}}{C_{\rm conv} + C_d + 2C_{oss}} \frac{L_{m,\rm pro}}{L_{m,\rm conv}} = 0.72. \tag{12}$$

$t_{\rm pro}$ and $t_{\rm conv}$ are the theoretical charging time using the proposed design methodology and the conventional one with frequency sweep results in Tab. I. It is shown that the charging time is reduced: $t_{\rm pro} = 400 \times 0.72 = 298ns$, which agrees with the measured results ($t_{\rm pro,m} = 300ns$). Therefore, the experimental prototype exhibits a reduction in the transformer lumped capacitance in both frequency sweep and the commutation performance.

V. Conclusion

In this paper, a methodology to reduce the lumped winding capacitance in spiral winding LLC transformer is proposed. The spiral winding lumped winding capacitance is modeled and analyzed. Both inter-winding and intra-winding capacitance are taken into consideration. Methods to calculate and to reduce the lumped capacitance is discussed. An experiment is designed to validate the proposed concept in both frequency sweep and commutation performance. Compared with the conventional method, the proposed design methodology can reduce the lumped windings capacitance from 14.40pF/turn to 1.76pF/turn in the experiments.

References

[1] M. A. Saket, N. Shafiei, and M. Ordonez, "LLC Converters with Planar Transformers: Issues and Mitigation," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4524–4542, Jun. 2017.

[2] C.-O. Yeon, J.-W. Kim, M.-H. Park, I.-O. Lee, and G.-W. Moon, "Improving the light-load regulation capability of llc series resonant converter using impedance analysis," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7056–7067, Sep. 2017.

[3] M. A. Saket, N. Shafiei, M. Ordonez, M. Craciun, and C. Botting, "Low parasitics planar transformer for LLC resonant battery chargers," *IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 854–858, May 2016.

[4] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant converters—a review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[5] F. Blache, J.-P. Keradec, and B. Cogitore, "Stray capacitances of two winding transformers: equivalent circuit, measurements, calculation and lowering," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meet.* IEEE, Oct. 1994, pp. 1211–1217.

[6] H. Y. Lu, J. G. Zhu, and S. Y. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1105–1112, Sep. 2003.

[7] L. Dalessandro, S. Member, S. Cavalcante, S. Member, J. W. Kolar, and S. Member, "Self-Capacitance of High-Voltage Transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2081–2092, Sep. 2007.

[8] M. Pahlevaninezhad, D. Hamza, and P. K. Jain, "An improved layout strategy for common-mode EMI suppression applicable to high-frequency planar transformers in high-power dc/dc converters used for electric vehicles," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1211–1228, Mar. 2014.

[9] C. Fei, Y. Yang, Q. Li, and F. C. Lee, "Shielding technique for planar matrix transformers to suppress common-mode emi noise and improve efficiency," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1263–1272, Feb. 2018.

[10] M. A. Saket, M. Ordonez, M. Craciun, and C. Botting, "Common-Mode Noise Elimination in Planar Transformers for LLC Resonant Converters," *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, pp. 6607–6612, Sep. 2018.

[11] Z. Ouyang, O. C. Thomsen, and M. A. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012.