H5-Bridge-Based Single-Input–Dual-Output *LLC* Converter With Wide Output Voltage Range

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***Abstract*—In this article, a novel single-input–dual-output *LLC* converter is proposed for wide output voltage applications. An H5-bridge is utilized on the primary side and linked with two separate resonant tanks. By morphing the H5 bridge, the input of each resonant tank can be configured as either full-bridge, half-bridge, or idle. On the secondary-side, two semiactive rectifiers provide two control degrees of freedoms. The circuit operation is always tuned at the optimal resonant frequency and the output voltages are modulated by the secondary side pulsewidth. It exhibits good voltage regulation performance with two fully decoupled output ports. Both output ports can achieve wide voltage ranges. All MOSFETs can achieve zero voltage switching turning-ON and all the diodes can achieve zero current switching turning-OFF over a wide output voltage and load ranges. To verify this concept, a 1.6-kW rated prototype is designed to convert 390-V input into two decoupled 100–400 V outputs. The designed prototype exhibits 97.72% peak efficiency and good decoupled voltage regulation performances. The experimental results agree well with the theoretical analysis.**

***Index Terms*—Dual-output converter, H5 bridge, *LLC*, pulsewidth modulation (PWM), wide voltage range.**

I. Introduction

IN APPLICATIONS such as multioutput programmable dc power supplies, integrated battery chargers, and multichannel LED drivers [1]–[3], multiple dc outputs are required with a wide output voltage range. A straightforward way to generate multiple outputs is to utilize multiple single-input–single-output (SISO) converters. Compared with multiple SISO converters [4], integrated single-input–multiple-output (SIMO) converter exhibits superior advantages such as fewer components, reduced cost, and higher power density [5]–[7]. Single-input–dual-output (SIDO) converter is the simplest SIMO converter with wide applications. To generate two independent outputs, the two output modules need to be regulated in a decoupled manner.

Among various SIDO converters, *LLC*-based SIDO converters draw wide research attention due to its attractive features such as galvanic isolation zero voltage switching (ZVS) for primary side MOSFETs, zero current switching (ZCS) for secondary-side diodes, and simple structure [8], [9]. For traditional *LLC* converter, pulse frequency modulation (PFM) is used to regulate the output voltage. However, PFM-based *LLC* converter is unable to generate two decoupled outputs due to cross regulation issues. Alternative modulation methods for *LLC* converter with fixed frequency are proposed such as primary-side pulsewidth modulation (PWM) [10], primary-side phase shift modulation (PSM) [11], secondary-side PWM [12], secondary-side PSM [13]–[15], and resonant frequency modulation [16], [17]. Those modulation methods provide additional control degree of freedom (DoF) for SIDO converters.

Generally, the modulation strategies for *LLC*-based SIDO converter can be classified into three categories. The first category is based on synchronous control with one control DoF [3], [18]. In [3], a multichannel constant-current *LLC* resonant LED driver is proposed. In [18], a dual-output *LLC* converter with wide input voltage range is proposed. Only PFM is utilized and both output ports are regulated simultaneously. Consequently, both ports are fully coupled and the issue of cross regulation occurs. This type of multiple-output control is not suitable for the applications that require decoupled control of each channel.

The second category is based on master and slave control [7], [19]. To ensure each channel independently regulated, the required control DoFs should be no less than the number of the outputs. In [7], a novel complementary PWM and PFM strategy is proposed. The master output is regulated by the duty cycle of the primary-side switches while the slave output is regulated by frequency. In [19], by regulating the phase-shift angle and the switching frequency, each channel can be regulated separately. However, these control variables are still coupled. When the master port voltage is being modulated, the slave port voltage is also affected. Cross regulation problem still exists with complicated control.

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The third category is based on independent control [20], [21]. In [20], a dual-output *LLC* resonant converter with magnetic control is proposed. Variable resonant inductance is enforced to adjust the resonant frequency of *LLC* tank to regulate the output voltages. Two outputs can be regulated by two independent resonant frequencies. However, the output voltage range is limited. In [21], *LLC* resonant converter and phase-shift-full-bridge (PSFB) converter are hybridized to achieve a SIDO converter. The output voltage of the *LLC* resonant converter is modulated by the switching frequency, while the output voltage of the PSFB converter is modulated by the phase angle. Therefore, the two output voltages are regulated independently and free from cross regulation.

The literature survey indicates that although different *LLC*-based SIDO topologies and modulation schemes have been investigated, there is still a lack of systematic solution to produce two decoupled outputs with ultrawide output voltage ranges. In [22] and [23], a five switches inverter bridge structure is proposed to extend the output voltage range of *LLC* converter. By reconfiguring the inverter bridge, a much wider output range can be achieved. However, PFM is used to regulate the output voltage, which makes it unsuitable to generate dual outputs with decoupled control.

The main novelties and contributions of this study are summarized as follows. First, a novel H5-bridge-based SIDO *LLC* converter is proposed. An ultrawide output voltage range can be achieved by configuring the primary-side H5 bridge and modulating the secondary-side pulsewidth. Second, the operation principles in different modes are analyzed in time domain and by trajectory tool. Third, elaborate design guidelines are provided to ensure wide ZVS range and improve efficiency. Fourth, based on various operation modes, corresponding control strategy is proposed to regulate dual independent outputs.

The benefits of the proposed topology include: Wide output voltage ranges; wide ZVS range for all MOSFETs and ZCS for all diodes; fewer components with reduced hardware cost compared with dual traditional SISO *LLC* converters with wide output voltage range [10], [22], [23]; two fully decoupled outputs; and easy design of magnetic components. Moreover, large magnetizing inductance can be selected, which effectively suppresses the circulating current.

This manuscript is organized as follows: Section II describes the proposed converter and its operation principles. Section III shows the theoretical analysis of the proposed converter. The key design considerations are presented in Section IV. The loss analysis and performance comparison are presented in Section V. The control strategy is shown in Section VI. Section VII demonstrates the experimental results. Finally, Section VIII concludes this article.

II. Topology and Basic Operation Principles

A. Topology Description

Fig. 1 shows the schematic of the proposed SIDO *LLC* topology. The primary side is a reconfigurable H5 bridge with five MOSFETs. The H5 bridge generates two high-frequency square waves, v_{ab} and v_{cb}. There are two sets of *LLC* resonant tank and rectifier. Those two resonant tanks are fully decoupled. The resonant tank parameters include resonant inductance (L_r), resonant capacitance (C_r), magnetizing inductance (L_m), and transformer turns ratio (n). The parameters of each resonant tank can be designed independently based on the characteristics of the desired output. The resonant frequencies between C_r and L_r in two resonant tanks are identical. The frequencies of v_{ab} and v_{cb} are tuned to be equal to the resonant frequency. On the secondary side, there are two independent semiactive rectifiers. The output voltage can be regulated by modulating the pulsewidth of secondary-side MOSFETs.

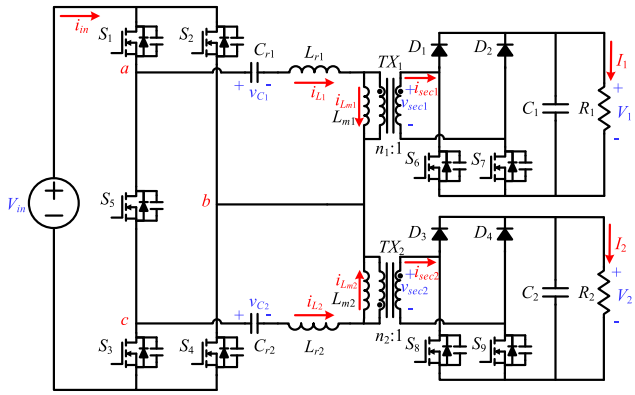

Fig. 1. Schematic of the proposed SIDO *LLC* topology.

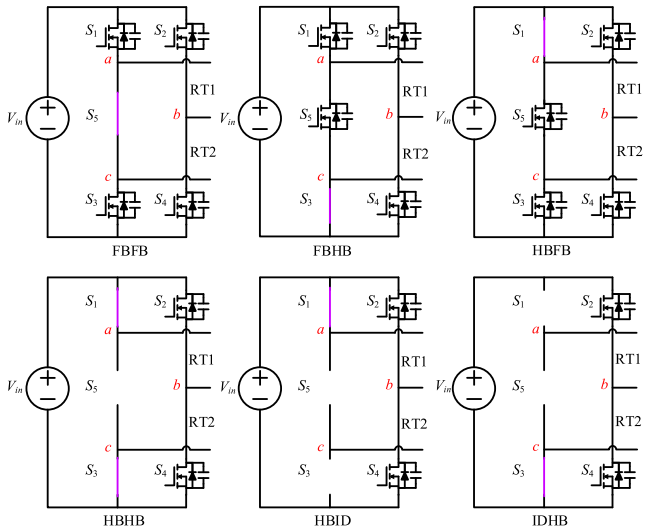

Fig. 2. Configurations of the H5 bridge.

B. Operation Principles

According to the configuration of the H5 bridge, there are six operating modes as shown in Fig. 2. The inputs of two resonant tanks (RT1 and RT2) can be configured as full-bridge (FB) mode, half-bridge (HB) mode, and idle (ID) mode. Therefore, six possible operating modes can be named as FBFB, FBHB, HBFB, HBHB, HBID, and IDHB based on the combination of two resonant tanks. The specific configuration and characteristics are summarized in Table I. $v_{\rm rms}$ means the rms value of the resonant

TABLE I
OPERATING MODES OF H5 BRIDGE

	RT	Mode	Voltage	v_{rms}	Switches
FBFB	RT1	FB	$v_{ab}: \pm V_{in}$	V_{in}	S_5 ON
	RT2	FB	$v_{cb}: \pm V_{in}$	V_{in}	
FBHB	RT1	FB	$v_{ab}: \pm V_{in}$	V_{in}	S_3 ON
	RT2	HB	$v_{cb}: -V_{in} \sim 0$	$V_{in}/2$	
HBFB	RT1	HB	$v_{ab}: 0 \sim V_{in}$	$V_{in}/2$	S_1 ON
	RT2	FB	$v_{cb}: \pm V_{in}$	V_{in}	
HBHB	RT1	HB	$v_{ab}: 0 \sim V_{in}$	$V_{in}/2$	$S_{1,3}$ ON
	RT2	HB	$v_{cb}: -V_{in} \sim 0$	$V_{in}/2$	S_5 OFF
HBID	RT1	HB	$v_{ab}: 0 \sim V_{in}$	$V_{in}/2$	S_1 ON
	RT2	ID	N/A	N/A	$S_{3,5}$ OFF
IDHB	RT1	ID	N/A	N/A	S_3 ON
	RT2	HB	$v_{cb}: -V_{in} \sim 0$	$V_{in}/2$	$S_{1,5}$ OFF

tank's input voltage. In the FB mode, $v_{\rm rms}$ is twice as much as that in HB mode. Therefore, the voltage gain in FB mode is doubled compared with that in HB mode. When one output port works in no-load condition, the corresponding resonant tank can operate in idle mode. Therefore, the appropriate operation mode can be selected based on the desired output voltages. It should be noted that HBID mode and IDHB mode are only suitable for the condition when only one output delivers power in half-bridge mode. The other output stays in idle mode. Compared with HBHB Mode, one more MOSFET is kept OFF. If only one full-bridge input is needed, FBFB Mode can be selected.

III. THEORETICAL ANALYSIS

A. Steady-State Analysis

There are six operation modes and two outputs are mutually independent. To simplify the theoretical analysis, only the first port of FBFB mode is analyzed in detail. The other port and the other operation modes can be analyzed similarly. The switching frequency is always tuned at the resonant frequency between L_r and C_r.

The key waveforms of FBFB mode are plotted in Fig. 3. For each secondary-side output, the secondary-side MOSFETs (S_6 and S_7, S_8 and S_9) are regulated by duty cycles as shown in Fig. 3. The duty cycles d for each branch are identical and are always equal to or greater than 0.5. They are driven in an interleaving manner with 180° phase difference. $v_{gs7,9}$ ($v_{gs6,8}$) are in phase with $v_{gs1,4}$ ($v_{gs2,3}$). The duty cycles of secondary-side MOSFETs are utilized to regulate the output voltages. It should be noted that when $d = 0.5$, secondary-side MOSFETs function as synchronous rectifier switches. This branch operates like a traditional *LLC* converter. The critical steady-state waveforms with duty cycle d_1 and d_2 are shown in Fig. 3. As shown in Fig. 3, the steady-state circuit operation can be divided into twelve operation stages. Fig. 4 shows the equivalent circuits of the six stages over a half switching cycle and the next six stages are symmetrical. The input current of the converter is equal to the sum of i_{L1} and i_{L2} in the positive half cycle. The input current of negative half cycle is equal to that of positive half cycle. When only considering the operation of the first output, four main parts can be divided and they are analyzed in detail

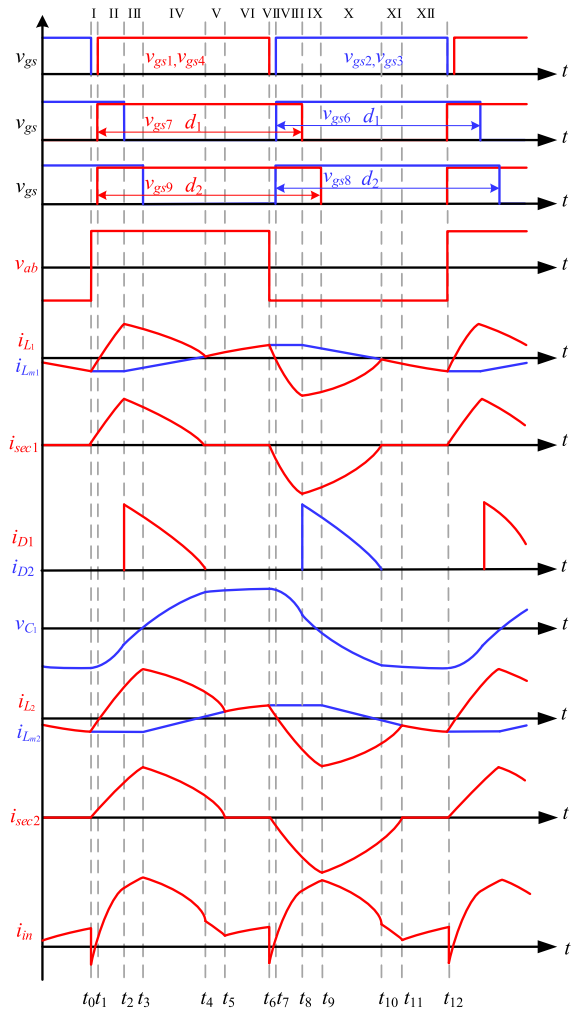

Fig. 3. Critical steady-state waveforms.

in the following. The operation principles of the second output are similar and can be derived easily.

Stage I: (t_0-t_1)[see Fig. 4(a)], before t_0, $S_{2,3}$ are ON, $S_{1,4}$ are OFF and the secondary side is an open circuit. On the primary side, L_{m1} resonates with L_{r1} and C_{r1}. At t_0, $S_{2,3}$ are turned OFF. At this moment, $i_{L_{r1}}$ is negative, which charges $C_{\rm oss}$ of $S_{2,3}$ and discharges $C_{\rm oss}$ of $S_{1,4}$. The freewheeling current discharges the parasitic output capacitance ($C_{\rm oss}$) of S_7. These negative currents create a ZVS condition for the turning-ON of $S_{1,4}$ and S_7.

Stage II: (t_1-t_2)[see Fig. 4(b)], $C_{\rm oss}$ of $S_{1,4}$, S_7 is discharged to 0 V since $i_{L_{r1}}$ is negative before t_1. $C_{\rm oss}$ can only be discharged completely if enough dead-time is employed. At t_1, $S_{1,4}$, and S_7 are turned ON with ZVS. In this stage, L_{r1} resonates with C_{r1}. The secondary side of transformer TX_1 is shorted. Secondary side voltage $v_{\rm sec1}$ is clamped to 0 V. Due to the deadband is small, the impact of deadband can be ignored. According to the KVL and KCL of RT1

$$C_{r1}\frac{dv_{C1}}{dt} = i_{L1} \tag{1}$$

$$L_{r1}\frac{di_{L1}}{dt} + v_{C1} = V_{in} \tag{2}$$

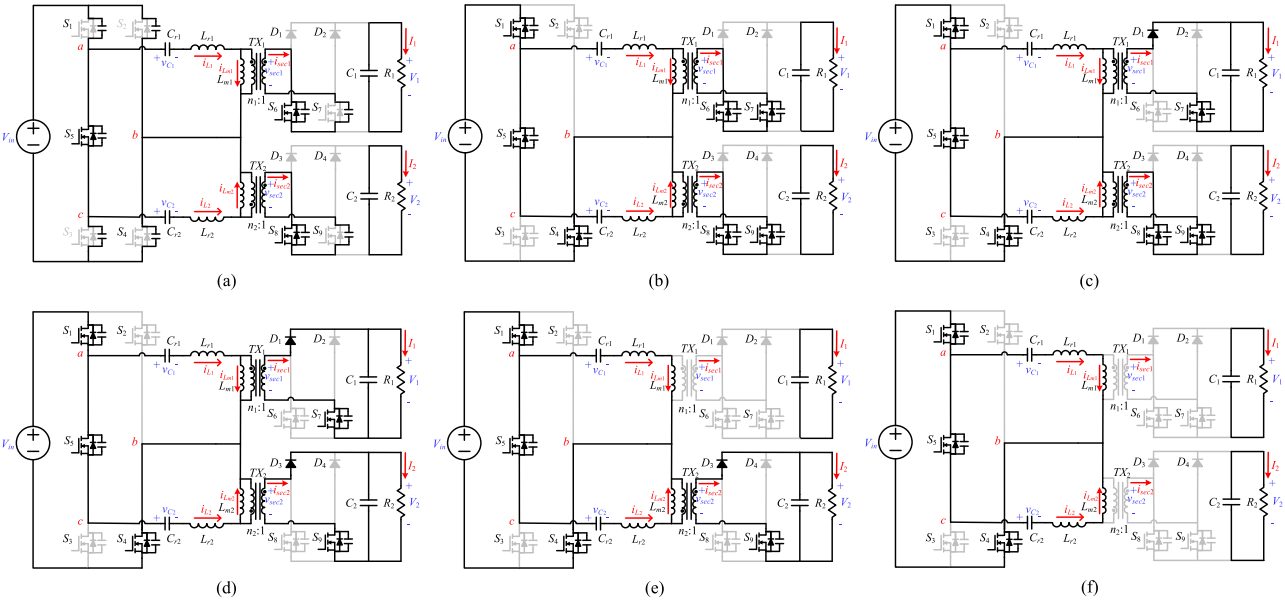

Fig. 4. Equivalent circuits over half switching cycle. (a) Stage I, $t_0 < t \le t_1$. (b) Stage II, $t_1 < t \le t_2$. (c) Stage III, $t_2 < t \le t_3$. (d) Stage IV, $t_3 < t \le t_4$. (e) Stage V, $t_4 < t \le t_5$. (f) Stage VI, $t_5 < t \le t_6$.

the time domain expressions of inductor current and capacitor voltage can be derived in Stages I and II

$$i_{L_1}(t) = i_{L_1}(t_0)\cos[\omega_1(t-t_0)] + \frac{V_{in} - v_{C_1}(t_0)}{Z_1}\sin[\omega_1(t-t_0)] \tag{3}$$

$$v_{C_1}(t) = i_{L_1}(t_0)Z_1\sin[\omega_1(t-t_0)] + (v_{C_1}(t_0) - V_{in})\cos[\omega_1(t-t_0)] + V_{in} \tag{4}$$

where
$\omega_1 = 1/\sqrt{L_{r1}C_{r1}}$, $Z_1 = \sqrt{L_{r1}/C_{r1}}$.

Stage III–IV: (t_2-t_4] [see Fig. 4(c)–(d)], S_7 remains ON while S_6 is turned OFF. Rectification diode D_1 freewheels the current i_{sec1}. v_{sec1} is clamped at V_1. At the end of this stage, the current of S_7 and D_1 drops to zero. S_7 and D_1 stops conduction. ZCS turning-OFF is realized for the secondary-side diode D_1. Therefore, the resonant current and voltage of RT1 during stages III–IV can be derived as follows:

$$i_{L_1}(t) = i_{L_1}(t_2)\cos[\omega_1(t-t_2)] + \frac{V_{in} - n_1V_1 - v_{C_1}(t_2)}{Z_1}\sin[\omega_1(t-t_2)] \tag{5}$$

$$v_{C_1}(t) = i_{L_1}(t_2)Z_1\sin[\omega_1(t-t_2)] + V_{in} - n_1V_1 + (v_{C_1}(t_2) - V_{in} + n_1V_1)\cos[\omega_1(t-t_2)]. \tag{6}$$

The magnetizing current of TX_1 ($i_{L_{m1}}$) increases linearly in stages III–IV. It can be expressed as

$$i_{L_{m1}}(t) = i_{L_1}(t_2) + \frac{n_1V_1}{L_{m1}}(t-t_2). \tag{7}$$

Stage V–VI: (t_4-t_6][see Fig. 4(e)–(f)], there is no rectification current on the secondary side of TX_1. C_{r1} resonates with L_{r1} and L_{m1} until the end of this half cycle. The resonant current and voltage of RT1 can be expressed as

$$i_{L_1}(t) = i_{L_{m1}}(t) = i_{L_1}(t_4)\cos[\omega_2(t-t_4)] + \frac{V_{in} - v_{C_1}(t_4)}{Z_2}\sin[\omega_2(t-t_4)] \tag{8}$$

$$v_{C_1}(t) = i_{L_1}(t_4)Z_2\sin[\omega_2(t-t_4)] + (v_{C_1}(t_4) - V_{in})\cos[\omega_2(t-t_4)] + V_{in} \tag{9}$$

where
$\omega_2 = 1/\sqrt{(L_{r1}+L_{m1})C_{r1}}$, $Z_2 = \sqrt{(L_{r1}+L_{m1})/C_{r1}}$.

It should be noted that compared with traditional secondary-side phase shift modulation method [13], the adopted secondary-side PWM control demonstrates reduced body diode conduction time. Therefore, conduction loss is reduced and efficiency can be improved.

B. Trajectory Analysis

The trajectory tool is employed to describe different operations to simplify the analysis. Define $v'_{C_1N}(t)$ and $i'_{L_1N}(t)$ as follows:

$$v'_{C_1N}(t) = \frac{v'_{C_1}(t)}{V_{in}}, \quad i'_{L_1N}(t) = \frac{i'_{L_1}(t)Z_1}{V_{in}}. \tag{10}$$

Based on (3)–(10), the trajectories of RT1 in different operation stages are plotted in Fig. 5. Fig. 5(a) and (c) show the trajectory waveforms in FB mode and HB mode with 50% secondary-side duty cycle, respectively. They are same to the traditional *LLC* converter operating in resonant frequency point. Fig. 5(b) and (d) illustrate the trajectory with more than 50% secondary-side duty cycle in FB and HB mode, respectively. In stages I–II of FB mode, the trajectory is a circle centered at (1, 0). The trajectory of RT1 is a circle centered at (1-G, 0) in stages

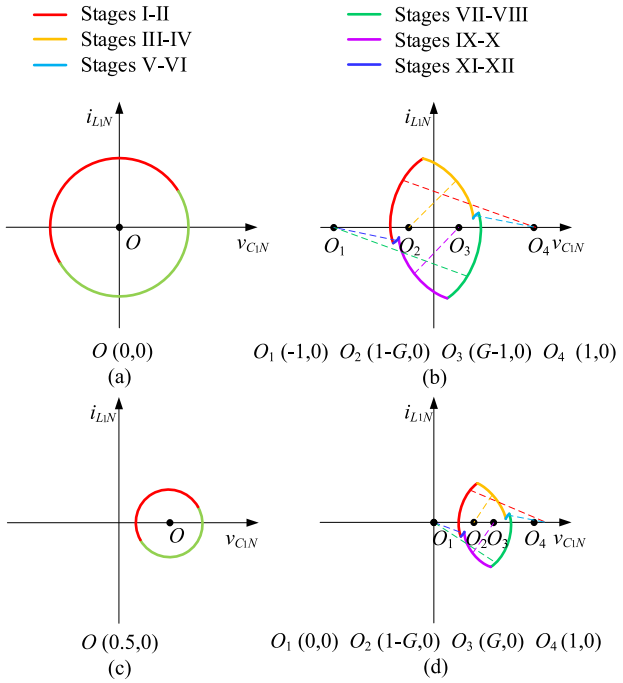

Fig. 5. Trajectory of RT1. (a) FB mode with 50% secondary-side duty cycle. (b) FB mode with more than 50% secondary-side duty cycle. (c) HB mode with 50% secondary-side duty cycle. (d) HB mode with more than 50% secondary-side duty cycle.

III–IV, where G is the normalized voltage gain. The normalized voltage gain G is defined as $G = n_1 V_1 / V_{in}$.

In stages V–VI, L_{m1} resonates with L_{r1} and C_{r1} and the input voltage of the resonant tank is V_{in}. Hence, the trajectory is an ellipse centered at (1, 0). Since stages VII–XII are symmetric to stages I–VI, the trajectory of other stages is similar to that of stages I–VI. Similarly, the trajectory in HB mode can be derived as shown in Fig. 5(d). Compared with FB mode, there exists a dc bias for the resonant capacitor voltage.

C. Voltage Gain Analysis

Although there are two independent outputs, the operating principles for each output port are identical. Consequently, only the voltage gain of one port in FB mode is analyzed. To simplify the analysis, the impact of deadband on voltage gain G is neglected.

The voltage gain can be increased by regulating the secondary-side duty cycle. In this situation, the converter operates like an isolated boost converter in discontinuous mode. The resonant inductor is charged when the secondary side of the transformer is shorted. Then, the current of the resonant inductor can be released to the output port through rectifier. The output voltage is raised like traditional boost converter.

The resonant frequency of f_r can be derived as

$$f_r = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}}. \tag{11}$$

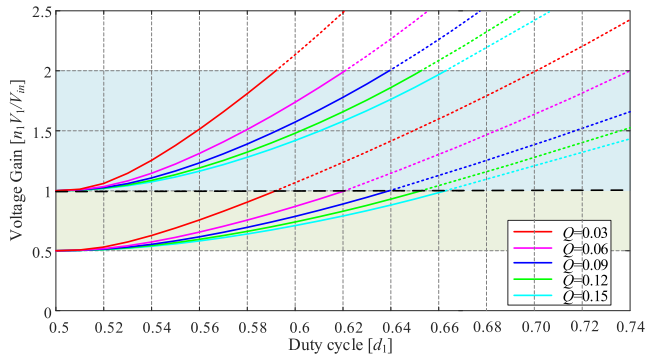

Fig. 6. Voltage gain curves versus d_1 under different Q.

Q is the normalized quality factor and L_n is the inductance ratio. They can be defined as

$$Q = \frac{\sqrt{L_{r1}/C_{r1}}}{{n_1}^2 R_1} \tag{12}$$

$$L_n = L_{m1}/L_{r1}. \tag{13}$$

Moreover, there are more restrictions on time domain analysis. Since stages VII–XII are symmetric to stages I–VI, we can get the following equations:

$$i_{L_1}(t_0) = -i_{L_1}(t_6) \tag{14}$$

$$v_{C_1}(t_0) = -v_{C_1}(t_6). \tag{15}$$

The magnetizing current is equal to resonant current at t_4

$$i_{L_1}(t_4) = i_{L_{m1}}(t_4). \tag{16}$$

The duty cycle of the S_7 and S_9, d_1 can be expressed as

$$d_1 = 0.5 + \frac{t_2 - t_1}{T_s} \tag{17}$$

where T_s is the switching period.

During the first half cycle, based on the power conservation law, we can obtain

$$2fV_{in}\int_{t_0}^{t_6} i_{L_1}(t)\,dt = \frac{V_1^2}{R_1}. \tag{18}$$

Combining (3)–(9), (11)–(18), the normalized voltage gain can be solved numerically by MATLAB for a given d_1 with Q and L_n. Similarly, the voltage gain in half-bridge mode can also be derived, which is half of that in full-bridge mode. For the proposed *LLC* converter, L_m should be designed as large as possible to suppress the circulating current. Fig. 6 demonstrates the calculated results of voltage gain versus duty cycle. As shown, the normalized voltage gain is designed to be in the range of [0.5, 2]. The whole normalized voltage gain can be divided into two segments. In half-bridge mode, the normalized voltage gain range is [0.5, 1]. Whereas, in full-bridge mode, the normalized voltage gain range is [1, 2]. In each mode, the normalized voltage gain is regulated by d_1. A larger duty cycle results in higher voltage gain in the same load condition. When $d_1 = 0.5$, the proposed converter is similar to a conventional *LLC* converter. Therefore, we can get the continuous output

voltage gain in the range of [0.5, 2] for all load conditions by adjusting d_1. According to Fig. 6, to achieve the same voltage gain, higher duty cycle is needed for heavier load condition. As a result, maximum voltage gain and full load condition should be taken into consideration when designing the resonant tanks.

The analytical expression of voltage gain in FB mode can be derived by ignoring the magnetizing inductance with similar modulation methods [13]. However, the analytical expression is complex and lacks accuracy. Therefore, the numerical solution is calculated in this manuscript. It is more accurate than the traditional approximate expression.

IV. Key Design Considerations

The specifications of the designed converter are summarized as follows: Input voltage V_{in}: 390 V; output voltage V_{o1}, V_{o2}: 100–400 V; output current I_{o1}, I_{o2}: 0.5–2 A; switching frequency f_s: 100 kHz.

The main design considerations are as follows. First, the resonant inductance and resonant capacitance are designed to suppress the current stress and meanwhile to satisfy the ZVS condition. Second, the magnetizing inductance is designed to fulfill the ZVS requirement of the primary-side MOSFETs.

A. Transformer Turns Ratio

In HF mode, the designed output voltage is 100–200 V. In FB mode, the designed output voltage is 200–400 V. The unity gain operating point is designed when output voltage equals 200 V in FB mode. Hence, the transformer turns ratio can be calculated as

$$n = \frac{390\text{V}}{200\text{V}} = \frac{39}{20}. \tag{19}$$

B. Resonant Inductance and Capacitance

The design consideration of L_r and C_r is to suppress the peak current with a secure ZVS. According to (11), large resonant inductance corresponds to small resonant capacitance when the resonant frequency is fixed. For different parameters of resonant tank, the peak resonant current is different. Since L_m is much larger than L_r, the peak current is insensitive to the L_m. The profiles of peak current versus output voltage under different Q are plotted in Fig. 7 when the load resistance is 100Ω, $L_{m1} = 700\mu$H. As shown in Fig. 7, the peak current increases with the output voltage for same Q. Moreover, higher Q corresponds to higher resonant inductance. The peak current is reduced and the loss can be decreased. However, too large Q can induce ZVS loss in high voltage gain condition as shown in Fig. 7. The magnetizing current in t_0 is positive to leave the ZVS region. Take RT1 as an example, the inductor current i_{L1} is very small during (t_4, t_6]. Therefore, the voltage of C_{r1} is charged slowly and it can be assumed as constant as $v_{C_1}(t_4)$ in (t_4, t_6]. Moreover, the magnetizing inductance is much larger than resonant inductance for same load condition. Therefore, the magnetizing current can be assumed to increase linearly as

$$i_{L_{m1}}(t) = i_{L_1}(t) \approx \frac{V_{in} - v_{C_1}(t_4)}{L_{m1} + L_{r1}}(t - t_4). \tag{20}$$

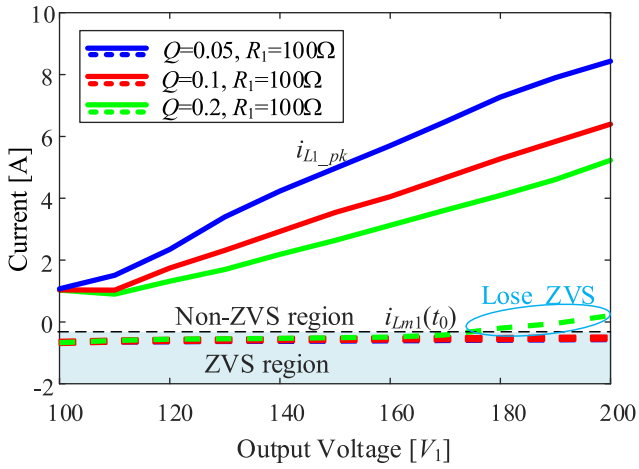

Fig. 7. Profiles of peak current and $i_{Lm1}(t_0)$ versus output voltage under different Q.

Large Q corresponds to small capacitance, which induces a large $v_{C_1}(t_4)$. It leads to a low magnetizing current at t_6, which may break the ZVS condition for primary-side MOSFETs. Therefore, the parameters of the resonant tank should be designed based on the tradeoff between secure ZVS range and low peak current. In our design, $L_{r1} = 46.9\mu$H and $C_{r1} = 54n$F are selected.

C. Magnetizing Inductance

The main design consideration of L_m is to satisfy the ZVS condition of primary-side MOSFETs. On the primary side, the H5 bridge is shared by two resonant tanks. Hence, the ZVS of primary-side MOSFETs is determined by both resonant tanks. As shown in Fig. 3, both $i_{L_{m1}}$ and $i_{L_{m2}}$ contribute to the ZVS realization of primary-side MOSFETs. As shown in Fig. 6, the normalized voltage gain for full-bridge mode is double compared with half-bridge mode for the same load condition and duty cycle. The amplitude of magnetizing current in half-bridge mode is only half of that in full-bridge mode. Therefore, the most vulnerable condition for ZVS is that one port operates in half-bridge mode while the other port is in idle mode. Consequently, the magnetizing current should be large enough to fully charge/discharge C_{oss} of MOSFETs to ensure the ZVS of primary-side MOSFETs in all operating modes. In this mode, the ZVS condition can be described as

$$i_{Lm1\_pk}, i_{Lm2\_pk} \geq \frac{2V_{in}C_{\text{oss}}}{t_d} \tag{21}$$

where t_d is the deadband between two MOSFETs in one bridge, and C_{oss} is the MOSFET parasitic output capacitance.

The peak magnetizing current can also be calculated numerically by Matlab in time domain. Fig. 8 discloses the profile of i_{L_m}'s peak current versus duty cycle with different load conditions and different L_m when the converter operates in single half-bridge mode. As we can see in Fig. 8, the amplitude of i_{Lm} decreases with the increase of duty cycle for the same load condition. For the same resonant tank and duty cycle, heavy load condition corresponds to low peak current. Meanwhile, large magnetizing inductance also results in low peak current.

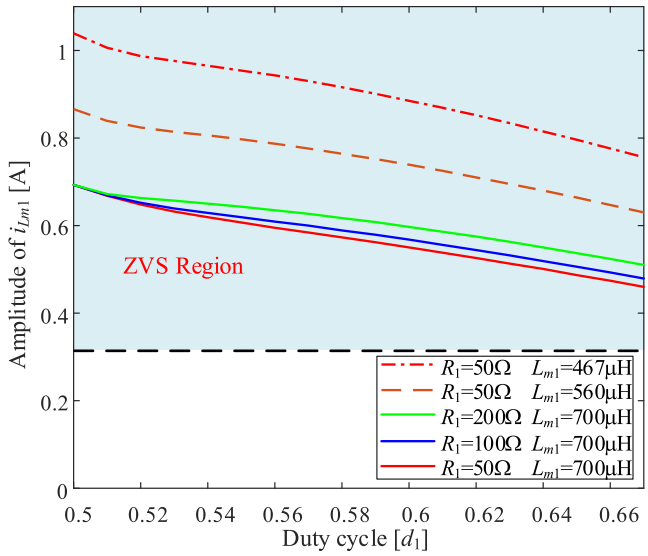

Fig. 8. Profiles of $i_{L_{m1}}$ versus duty cycle with different R_1 and L_{m1} when $L_{r1} = 46.9\mu$H and $C_{r1} = 54n$F.

The circulating current is reduced with narrowed ZVS range. As shown in (21), short deadband corresponds to high peak magnetizing current. While long deadband induces high duty cycle loss. Therefore, there is a tradeoff between magnetizing inductance and deadband. Moreover, short deadband may lead to the shoot through of the bridge arm. Proper time margin is necessary. Based on all these considerations, 100-ns deadband is adopted to ensure secure ZVS and to avoid shoot through. The corresponding magnetizing current condition with 100-ns deadtime is plotted in Fig. 8. Certain margin is reserved to ensure secure ZVS. Thus, magnetizing inductance can be designed to ensure the ZVS of primary-side MOSFETs. We choose $L_m = 700\mu H$ to achieve wide ZVS range and low circulating current.

V. Loss Analysis and Performance Comparison

A. Loss Analysis

The main losses can be divided into four parts: Conduction loss, transformer copper loss, transformer core loss, and switching loss. The conduction losses include MOSFET conduction loss, diode conduction loss, and capacitor conduction loss. The proposed converter can achieve ZVS turn-ON and diodes can achieve ZCS turn-OFF. Thus, the turn-ON loss of MOSFET and turn-OFF loss of diode are negligible. The switching loss mainly attributes to the MOSFET turn-OFF loss. The magnetic core loss can be estimated by Steinmetz's equation. According to the above analysis, the power losses in different voltages at heavy load condition are calculated and plotted in Fig. 9. The core loss is higher in FB mode than in HB mode. Some switching losses are induced by secondary-side extended duty cycle.

B. Performance Comparison

As reviewed in Section I, many SIDO *LLC* converters have been proposed. The comparison with state-of-the-art SIDO *LLC* topologies is summarized in Table II. In [18], PFM is adopted to regulate both outputs. Therefore, two outputs are coupled with one control variable. In [7] and [19], the number of control DoFs is equal to that of outputs. However, there exists cross regulation issue due to the coupling of control variables. In [20] and [21], the numbers of control variables and outputs are identical and the control variables are decoupled with each other. Therefore, two outputs are regulated independently and free from cross regulation. The proposed topology also has the advantage of independent control. Compared with the state-of-the-art SIDO *LLC* topologies, the output voltage range of the proposed converter is much wider. The numbers of MOSFETs and diodes are sacrificed to some extent to achieve wider output voltage ranges. However, compared with dual traditional SISO *LLC* converters with wide output voltage range [10], [22], [23], the number of components is reduced.

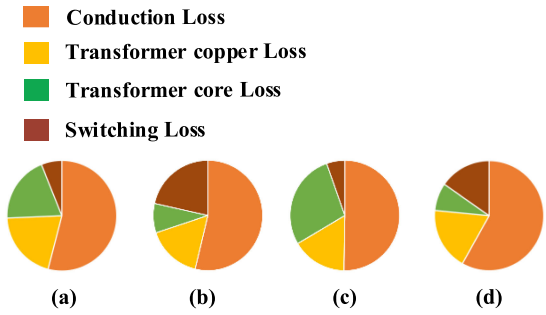

Fig. 9. Loss breakdown in different output voltages at heavy load condition.

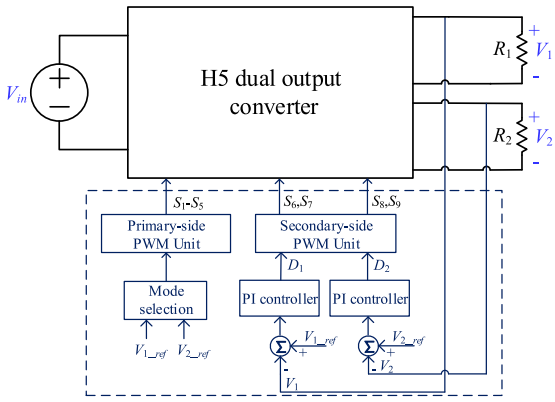

Fig. 10. Diagram of the digital control scheme.

VI. Control Strategy

The digital control scheme is plotted in Fig. 10. On the primary side, the configuration of the H5 bridge in Fig. 2 is selected based on the desired two output voltage ranges. The desired output voltages (V_{1_ref}, V_{2_ref}) are input to the DSP controller, each resonant tank can be classified into FB mode, HB mode, or ID mode. When the desired normalized voltage gain range is in [1, 2], the resonant tank operates in FB mode. The resonant tank operates in HB mode if the desired voltage is in [0.5, 1]. The output voltage can also operate in idle mode without load. Based on two

TABLE II
COMPARISON WITH EXISTING DUAL-OUTPUT *LLC* CONVERTERS

Topologies	Quasi Two-stage *LLC* [18]	*LLC* with extended PWM [19]	*LLC* with SAR [20]	*LLC* with variable inductance [21]	Hybrid modulation of *LLC* and FSFB [22]	Proposed
Modulation	PFM	PWM + PFM	PFM + PSM	Magnetic control	PSM + PFM	PWM
Number of MOSFETs	8	4	6	2	4	9
Number of diodes	0	8	4	8	6	4
Number of transformer	1(center-tapped)	2	2	2	3	2
Input Voltage	48V-85V	300V-330V	95V-105V	300V-380V	400V	390V
Output Voltage	12V-17V; 6V-8.5V	24V; 48V	28V; 42V	24V; 48V	200V-400V; 48V	100V-400V; 100V-400V
Number of control freedom	1	2	2	2	2	2
Control coupling	Yes	Yes	Yes	No	No	No
Power level	100W	480W	420W	200W	1200W	1600W
Peak efficiency (%)	95.1	94	96.6	N/A	95.3	97.72

TABLE III
PARAMETER OF COMPONENTS

Symbol	Quantity	Values
V_{in}	Input voltage	390V
V_1, V_2	Output voltages	100-400V
I_1, I_2	Output currents	0-2A
S_{1-9}	MOSFETs	SCT3120
D_{1-4}	Rectification diodes	C3D10060
$L_{r1,2}$	Resonant inductance	46.9μH
$C_{r1,2}$	Resonant capacitance	$54n$F
$L_{m1,2}$	Magnetizing inductance	700μH
$C_{1,2}$	Output capacitance	220μF
$n_{1,2}$	Transformer turns ratio	39 : 20
f_s	Switching frequency	$100k$Hz
$TX_{1,2}$	Magnetic core	PC95 EC4950

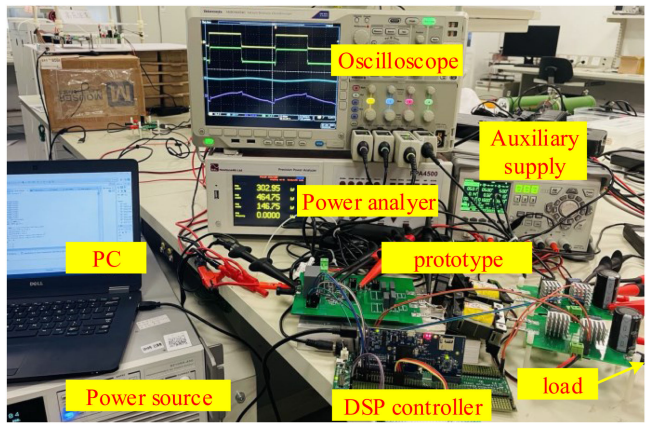

Fig. 11. Photograph of the laboratory test bench.

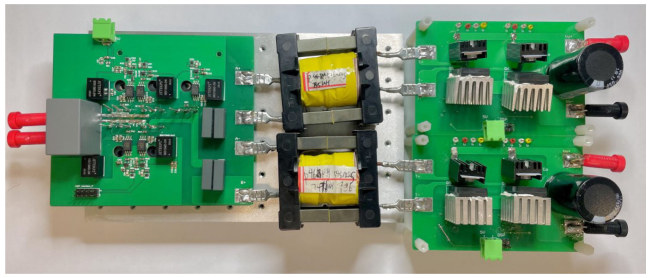

Fig. 12. Photograph of the designed SIDO *LLC* converter.

operating modes of two resonant tanks, the configuration of H5 can be chosen based on Table I. The operation of primary-side switches in different modes is also summarized in Table I. On the secondary sides, two duty cycles are regulated dynamically by two close-loop PI controllers. Two duty cycles are decoupled and two PI controllers are independent. The PWM unit generates the corresponding gate driving signals for the MOSFETs. Then, the output voltage is tightly regulated. This control strategy is simple and easy to be implemented.

VII. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed converter, a 1.6 kW/100 kHz prototype with 390-V input and dual 100–400-V outputs is designed. The key design parameters are summarized in Table III. Although two identical resonant tanks and transformers are designed to simplify the analysis, they can be designed independently based on the requirement of each output. The picture of the test bench is given in Fig. 11. The photograph of the power stage is shown in Fig. 12. TMS320F28379 from Texas Instrument is used to implement the digital control algorithms.

The steady-state experimental waveforms with different output voltages in full load condition are captured in Fig. 13. Fig. 13(a) shows the waveforms with two identical output profiles in FBFB mode with 50% secondary-side duty cycles. The experimental waveforms of the extreme condition $V_1 = V_2 = 400$ V are captured in Fig. 13(b)–(c). S_1 and S_7 are turned ON simultaneously. There is an extended conduction time for S_7 compared with S_1 as shown in Fig. 13(c). Fig. 13(d) demonstrates the steady-state waveforms in HBFB mode with 50% duty cycles. The first port operates in HB mode and the second port operates in FB mode. The effective voltage of v_{ab} is half of that of v_{cb}. Fig. 13(e) shows the steady-state waveforms with $V_1 = 150$ V and $V_2 = 250$ V. The converter operates in HBFB mode with two independent secondary-side duty cycles. The critical waveforms of another extreme operation condition of $V_1 = V_2 = 100$ V are captured in Fig. 13(f). Both resonant tanks operate in HB mode. The waveforms of diode voltages and currents are presented in Fig. 14. Fig. 14(a) shows the waveforms when the secondary-side duty cycle equals to 50%. The diodes operate like traditional *LLC* converter. Fig. 14(b)

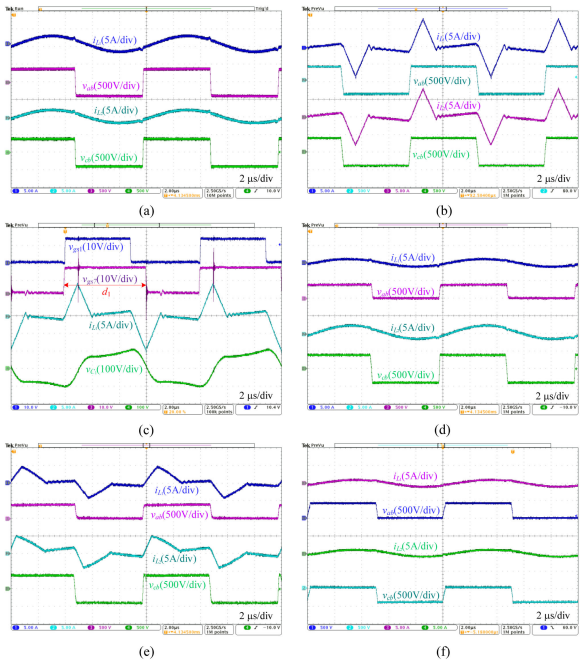

Fig. 13. Experimental steady state waveforms in different modes. (a) FBFB mode $V_1 = V_2 = 200$ V, $P_1 = P_2 = 400$ W. (b) FBFB mode $V_1 = V_2 = 400$ V, $P_1 = P_2 = 800$ W. (c) FBFB mode $V_1 = 400$ V, $P_1 = 800$ W. (d) HBFB mode $V_1 = 100$ V, $P_1 = 100$ W, $V_2 = 200$ V, $P_2 = 400$ W. (e) HBFB mode $V_1 = 150$ V, $P_1 = 300$ W, $V_2 = 250$ V, $P_2 = 500$ W. (f) HBHB mode $V_1 = V_2 = 100$ V, $P_1 = P_2 = 100$ W.

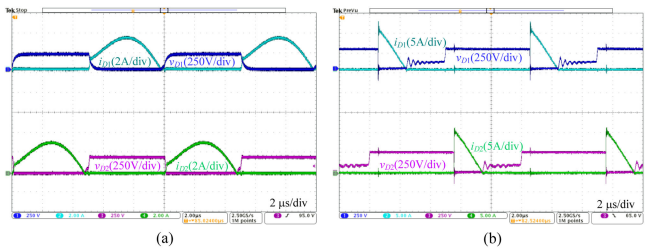

Fig. 14. Waveforms of diode voltages and currents when RT1 operates in FB mode with $I_1 = 2$ A. (a) $V_1 = 200$ V. (b)$V_1 = 250$ V.

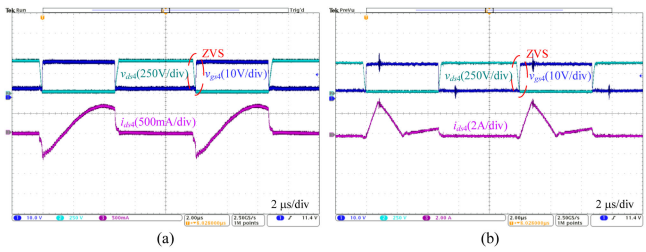

Fig. 15. Soft-switching waveforms of the primary-side MOSFET in HBID mode. (a) $V_1 = 100$ V. $P_1 = 50$ W. (b) $V_1 = 200$ V. $P_1 = 400$ W.

shows the waveforms of $V_1 = 250$ V. The secondary-side duty cycle is larger than 50%. ZCS turning-OFF of diodes can always be realized in all operation conditions.

The critical soft-switching waveforms are captured in Figs. 15 and 16. Fig. 15(a) exhibits the ZVS waveforms of primary-side MOSFETs in light load with $V_1 = 100$ V, $P_1 = 50$ W. As shown

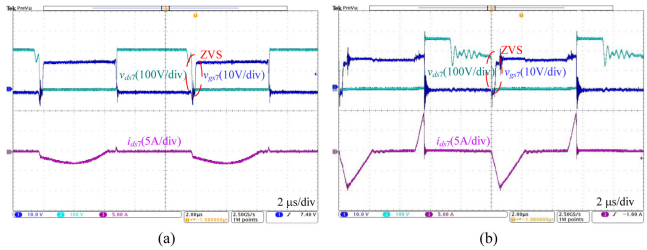

Fig. 16. Soft-switching waveforms of the secondary-side MOSFET with RT1 operating in FB mode. (a) $V_1 = 200$ V, $I_1 = 2$ A. (b) $V_1 = 250$ V, $I_1 = 2$ A.

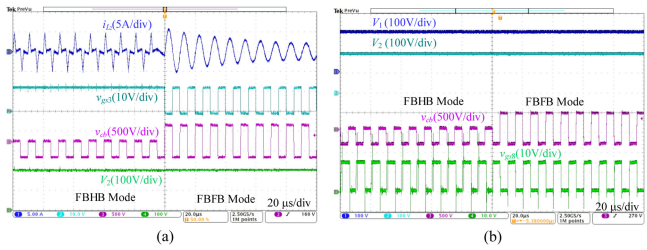

Fig. 17. Dynamic transition from FBHB Mode to FBFB Mode with $V_1 = V_2 = 200$ V, $P_1 = P_2 = 200$ W.

in Fig. 8, the worst ZVS condition is in heavy load condition of half-bridge mode with maximum secondary-side duty cycle. The ZVS waveforms in this worst ZVS condition are shown in Fig. 15(b). As shown in Fig. 15, there is no overlap between the rising edge of v_{gs} and the falling edge of v_{ds} in half-bridge mode, which validates the ZVS turning-ON of the primary side MOSFETs in the strictest situation. The negative current contributes to the ZVS turning-ON of the MOSFET. As a result, ZVS of primary-side MOSFETs in other operating modes can also be realized. Similarly, Fig. 16 proofs that ZVS is realized for the secondary-side MOSFETs when RT1 operates in FB mode. Fig. 16(a) shows the condition of 50% secondary-side duty cycles. The MOSFETs act as synchronous rectifier switches. Fig. 16(b) demonstrates the ZVS waveforms of 250-V output voltage. The negative current contributes to the ZVS realization of secondary-side MOSFETs. C_{oss} of MOSFETs resonates with the parasitic inductor when there is no freewheeling current on the secondary side.

Fig. 17 exhibits the dynamic transition of the second port from FBHB mode to FBFB mode. V_2 is kept as 200 V. S_5 starts to conduct constantly and S_3 starts being switched at the resonant frequency. v_{cb} changes from HF mode to FB mode. Thus, the effective voltage is doubled. As shown in Fig. 17(b), the secondary-side duty cycle is reset to 50% after the transition. V_1 is unaffected during the transition, which proves the decoupling feature of two outputs. A smooth transition is achieved without transient issues.

In order to verify the dynamic behavior of the proposed dual-output *LLC* converter, load transition experiment has been carried out. The experimental waveforms of the first port load step down from 250 to 150 W in 250 V are presented in Fig. 18. The transition is smooth and output voltage V_1 is well regulated. It shows that the proposed resonant converter exhibits good

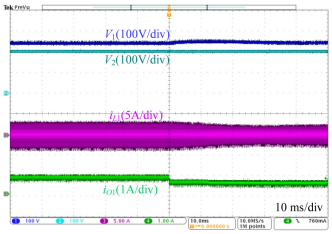

Fig. 18. Dynamic waveforms of load step down from 250 to 150 W.

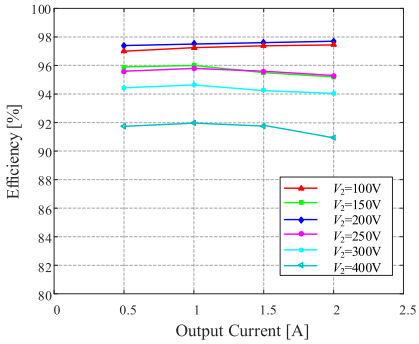

Fig. 19. Measured efficiency versus I_2 with different V_2 ($V_1 = 200$ V, $I_1 = 2$ A).

dynamic response performance. Output voltage V_2 is unaffected, which indicates the decoupling characteristic of two outputs.

Efficiency versus output current in dual-output condition with different output voltages is measured and plotted in Fig. 19. The output of the first port is kept as 200 V, 400 W. The second port operates with wide output voltage ranges and different load conditions. As shown, the prototype demonstrates good efficiency performance over the wide output voltage range. Peak efficiency can be achieved with $d_1 = 50\%$ both in full-bridge mode and half-bridge mode. The corresponding loss breakdown is shown in Fig. 9. In each operating mode, efficiency decreases with the increase of output voltage. That is because of the induced high peak current and high rms current. Both conduction loss and switching loss increase. Two independent wide output voltage ranges are achieved at the cost of sacrificed efficiency performance in high voltage gain condition. 97.72% peak efficiency is recorded when both ports operate in full-bridge mode.

VIII. Conclusion

In this article, a novel H5-bridge-based SIDO *LLC* converter is proposed for wide output voltage range applications. Six operation modes of the H5 bridge can be customized to suit the desired voltages of two output ports. The operating principles and theoretical analysis are detailed. The resonant frequency of two resonant tanks are designed to be identical. The switching frequency is matched to the resonant frequency, which facilitates a simplified design of the magnetic components. Two outputs can be regulated independently by two independent secondary-side duty cycles.

A 1.6-kW rated prototype with 390-V input and dual outputs was tested to verify the proof of concept. Each output exhibited an ultrawide voltage range as [100, 400 V]. Fully decoupled regulations of two outputs were achieved experimentally. Steady-state waveforms and ZVS waveforms are well illustrated. The peak efficiency is measured was 97.72%. Good efficiency and soft-switching performances over wide voltage and load ranges are recorded.

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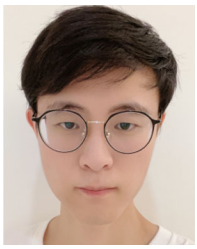

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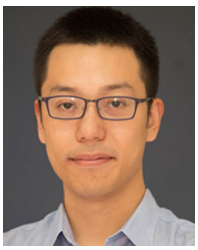

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