Universal Control Scheme to Achieve Seamless Dynamic Transition of Dual-Active-Bridge Converters Using Zero-Current-Prediction

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***Abstract*—This article proposes a zero-current-prediction based digital control scheme to achieve the seamless dynamic transition of dual-active-bridge (DAB) converters. Compared with existing methods, only an extra variable between the master pulsewidth modulation and the sawtooth carrier is introduced. This extra variable is only determined by the voltage conversion ratio and the change of the existing phase shifts between master and slave legs. It accurately predicts the zero crossings of the inductor current and tunes it with the end of the carrier period. When the output power varies, the controller updates the digital registers at the beginning of the new carrier period, when the inductor current is zero. Thus, a seamless dynamic transition is achieved with zero dc bias current. This proposed digital control scheme is universally valid for the mainstream modulation methods of a single DAB converter. Moreover, it is adaptive to any load conditions, regardless of the zero-voltage-switching conditions and power flow directions. A hardware prototype is designed, tested, and compared with the conventional control method. The experimental results well validate the advantages of the proposed concept.**

***Index Terms*—DC bias current, dual-active-bridge, modulation method, seamless dynamic transition, zero-current-prediction.**

Nomenclature

ZCP	Zero current prediction.
DAB	Dual-active bridge.
PWM	Pulsewidth modulation.
ZVS	Zero voltage switching.
SPS	Single-phase shift.
EPS	Extended phase shift.
DPS	Dual-phase shift.
TPS	Triple-phase shift.
VFM	Variable frequency modulation.
CMP_n	Compare register.
DSP	Digital signal processor.
TBPRD	Time base period register.
TBPHS	Time base phase register.
SYNCI	Synchronization signal.

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I. Introduction

DUAL-active-bridge (DAB) converter, first proposed by Doncker *et al.* [1] in 1991, is becoming a mainstream bidirectional isolated dc/dc topology in emerging applications such as electric vehicles, energy storage systems, and microgrids [2]–[5]. Fig. 1 illustrates the schematic of a typical DAB converter. There are two H-bridges which consist of four legs (L_1-L_4), each leg has two switches driven by complementary gate signals with 50% duty cycle. Typically, L_1 is defined as the master leg, while the phases of the other legs are shifted with respect to L_1. Single-phase-shift modulation (SPS) is a classic modulation method for the DAB converter. In SPS, the inner phase-shift in each H-bridge is $T_s/2$. The outer phase-shift (D_2T_s) between L_1 and L_3 can be utilized to regulate the direction and amount of the power [6], [7]. For better steady-state performance such as wider zero-voltage-switching (ZVS) range and higher efficiency under different conditions, extended phase-shift (EPS) [8], [9], dual phase-shift (DPS) [10], [11], triple phase-shift (TPS) [12]–[14], and variable-frequency (VFM) modulation [15]–[17] are proposed within two additional inner phase shifts (D_1T_s, D_3T_s) in each H-bridge or variable switching frequency.

The dynamic response is crucial for the DAB converter as it affects the system reliability [18]–[20]. However, the dc-bias current in the inductor is a main challenge during the transients [21]. It may lead to magnetic saturation or even system failure. Connecting a dc-blocking capacitor in series with the transformer can avoid magnetic saturation. But this dc capacitor is usually bulky and incurs extra conduction loss.

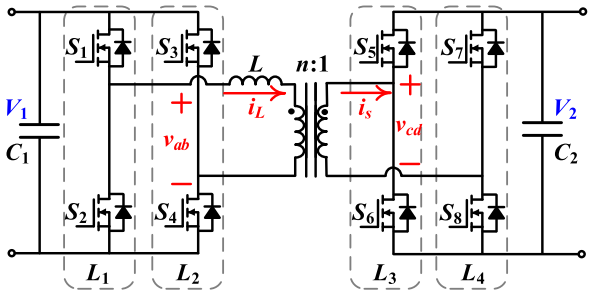

Fig. 1. Schematic of a typical DAB converter.

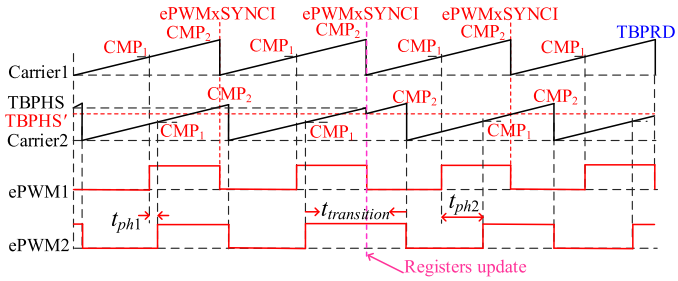

Fig. 2. Mechanism of switch pattern generation using the conventional method.

To eliminate this transient dc bias current, multiple phase-shifts modulation methods are investigated. In [21]–[23], the phase-shift of each leg is clearly derived. The dc-bias current is effectively eliminated. In [24], a fast recovery control is proposed by adjusting the gate signals of the secondary side simultaneously in a feedforward manner. The transient dc bias current can be effectively suppressed. In [25] and [26], predictive control solutions with current measurement are studied. In [27], a deadbeat current controller with enhanced SPS modulation is proposed to achieve a fast dynamic response. However, the current sensors and the required auxiliary circuitry increase the cost and complexity. In [28], an improved model based method is presented for three-phase DAB converter to mitigate the transient dc bias in the magnetizing flux. In [29] and [30], the dc bias current is eliminated by maintaining volt-second balance during the transient process. Besides, the transient ZVS is achieved in [31]. In [32], the DAB converter is modeled by four subcircuits to separately drive each half-bridge for volt-seconds balancing of the transition. In [33], a dedicated PWM generation technique is proposed to eliminate the dc bias current. In [34], a natural switching surface-based boundary control is studied to achieve fast transient. In [35], the optimization of transients with the TPS modulation is investigated.

The literature survey indicates that although the aforementioned methods can remove the dc bias current effectively, most of them only address ZVS conditions and require multiple updates of the register. Although Wei *et al.* [27] consider non-ZVS conditions, it is only applicable to SPS modulation and requires current measurement. Besides, there is no applicable solution for the dynamic response of VFM modulation.

In [36], the concept of shifting switching pattern to realize zero initial current in each switching cycle is proposed. However, only SPS combined with triangular and trapezoidal modulation are addressed. The implementation is based on a look-up table, which limits the universality and robustness.

To address this issue, this article proposes a zero-current-prediction (ZCP) based digital control scheme by introducing an extra control variable between the master PWM and the sawtooth carrier. The extra variable ensures that the inductor current is zero at the beginning and end of each carrier period. When the load changes, the registers are updated at the beginning of the following period. Then, the converter reaches the new state seamlessly. The transient dc bias current can be eliminated. This technique can be deployed to all mainstream modulation methods of single DAB converter and the registers only need to be updated once, which reduces the implementation complexity. Moreover, the proposed method does not require current measurement, the calculation is easy to implement, and the extra variable is independent of converter parameters.

The article is organized as follows. The generation mechanism of the dc bias current is analyzed in Section II. In Section III, the mainstream modulations of DAB are detailed with the proposed method. Section IV elaborates the design considerations in practical implementation. Experimental results are demonstrated in Section V for validation of the analysis. Finally, Section VI concludes this article.

II. Mechanism of the Dc-Bias

Fig. 2 depicts the generation mechanism of the driving signals using digital-signal-processor (DSP) controller. The carriers are sawtooth waves generated by the period counter. The counting period which is stored in the period register (TBPRD) determines the steady-state switching frequency. The compare registers CMP_1 and CMP_2 are separated by half the switching cycle, which determine the rising and falling edges of the gate signals. Typically, TBPRD, CMP_1, and CMP_2 of leg L_1 are fixed to a desired value ($\text{CMP}_2 = \text{TBPRD}$ in Fig. 2.), and the generated driving signal can be set as a master gate signal. While the gating signals of the other legs would be changed with respect to the fixed signal of L_1 according to the requirement.

The most common method of generating a phase shift angle is to use a phase register (TBPHS) in other carriers (e.g., carrier2). At the end of the counting period in carrier1, the counter is cleared. Meanwhile, a synchronization signal is issued to Carrier2 to force the counting value to be TBPHS. Then, a phase shift t_{ph} is generated between the gate signals ePWM1 and ePWM2. When the phase shift changes, the phase register is updated to TBPHS′ at the next synchronization signal. Then, the phase shift changes from t_{ph1} to t_{ph2}. The duty cycle is larger than 50% during the transition process.

Fig. 3 shows the key waveforms of the DAB converter when the load current increases in SPS modulation. The outer phase shift increases from t_{ph1} to t_{ph2}. The profile of primary side voltage v_{ab} remains unchanged, and the profile of secondary side voltage v_{cd} is shifted by $\Delta t_{ph} = t_{ph2} - t_{ph1}$. Therefore, the duration of the negative level on the secondary side becomes longer than half-cycle as analyzed above. It causes unbalanced volt-seconds and incurs a dc bias current to the inductor. In other

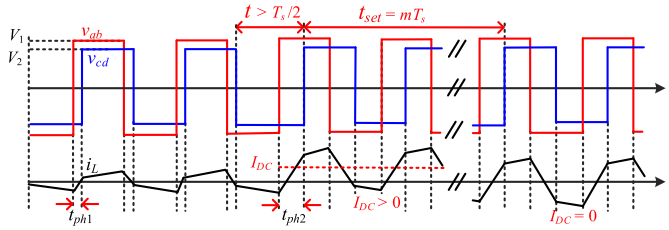

Fig. 3. Waveforms of DAB when the load current increases with the conventional SPS modulation.

modulation methods, the dc bias current also occurs due to the unbalanced volt-second. Although the dc bias current can be damped by the parasitic series resistance, the settling time t_{set} jeopardizes the dynamic response speed.

III. Analysis of the Proposed Control Scheme

In this article, an additional variable α is utilized to predict the zero current point. As analyzed in Section II, CMP_2 is the falling signal of the master leg, which determines the falling edge of the primary voltage v_{ab} from V_1 to zero. αTs is the time interval between CMP_2 and the zero point of the inductor current. Then, the zero current point is synchronized with the end of the carrier period to ensure a seamless dynamic transition. Besides, for a designed DAB converter, the power delivery is determined by the phase shifts among different phase legs. With the proposed method at steady state, the practical phase shifts will not be affected. The generated gate signals of the proposed method are identical to the conventional method. Therefore, the proposed method does not limit the output power level of the DAB converter. The efficiency of the system will not be affected either.

A. Analysis of ZCP-Based SPS Modulation

In the SPS modulation, the transferred power P is a function of the outer phase-shift ratio D_2

$$P = \frac{2nV_1V_2}{f_sL}D_2\left(\frac{1}{2} - |D_2|\right), D_2 = \frac{t_{ph}}{T_s} \tag{1}$$

where V_1 is the primary side port voltage, V_2 is the secondary side port voltage, n is the transformer turns ratio, f_s and T_s are the switching frequency and period, respectively, L is the inductance. There are two control variables (t_{ph} and α).

The normalized voltage conversion ratio is defined as

$$k = \frac{nV_2}{V_1}. \tag{2}$$

Due to the symmetrical structure, only buck mode is addressed, which means that the voltage conversion ratio $k < 1$. It should be noted the other cases can be analyzed similarly. According to different ZVS conditions and power flow directions, the operation of DAB with SPS modulation can be divided into four modes. α can be calculated correspondingly. For example, if the peak current of the inductor is I_p as shown in Fig. 4(a).

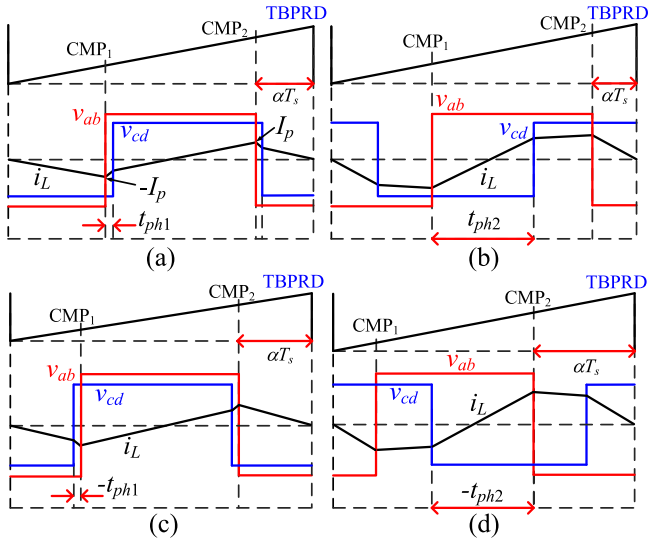

Fig. 4. Key waveforms of four modes in ZCP based SPS modulation, (a) non-ZVS in the forward direction, (b) ZVS in the forward direction, (c) non-ZVS in the backward direction, and (d) ZVS in the backward direction.

Then, the following equation stands:

$$-I_p + \frac{V_1 + nV_2}{L}D_2T_s + \frac{V_1 - nV_2}{L}(\frac{1}{2} - D_2)T_s = I_p \tag{3}$$

I_p can be calculated as

$$I_p = \frac{V_1 + nV_2}{2\,L}D_2T_s + \frac{V_1 - nV_2}{2\,L}(\frac{1}{2} - D_2)T_s. \tag{4}$$

According to the waveform of i_L, there are two stages from $-I_p$ to zero, one is the phase shift t_{ph1}, the other is $\alpha T_s - t_{ph1}$. Then, α can be calculated according to the following equation:

$$-I_p + \frac{V_1 + nV_2}{L}D_2T_s + \frac{V_1 - nV_2}{L}(\alpha - D_2)T_s = 0. \tag{5}$$

Consequently, α can be derived from (5). Correspondingly, α of the four different modes can be derived as

$$\alpha = \begin{cases} \frac{1-4D_2k-k}{4(1-k)}, Forward\ without\ ZVS \\ \frac{1+4D_2k-k}{4(1+k)}, Forward\ with\ ZVS \\ \frac{1-4D_2k-k}{4(1-k)}, Backward\ without\ ZVS \\ \frac{1+4D_2k+3k}{4(1+k)}, Backward\ with\ ZVS \end{cases} \tag{6}$$

α is only determined by D_2 and k. Therefore, it would not be affected if the converter parameters change. The ZVS and non-ZVS conditions are determined by the current direction when the switch turns ON. In the buck mode, the conditions of ZVS and non-ZVS can be derived with respect to k

$$\begin{cases} |D_2| \le \frac{1-k}{4}, & non-ZVS \\ |D_2| > \frac{1-k}{4}, & ZVS \end{cases}. \tag{7}$$

Practically, the phase shift ratio is calculated according to the desired transferred power P, V_1, and V_2. The proposed method only requires the controller to judge the ZVS condition and power flow direction after the calculation of the phase shift ratio. Fig. 4 depicts the key waveforms of the four modes. It shows that at the beginning and end of each carrier period, the inductor

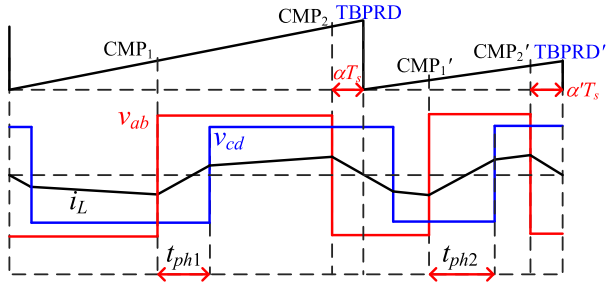

Fig. 5. Key waveforms of the ZCP based VFM modulation.

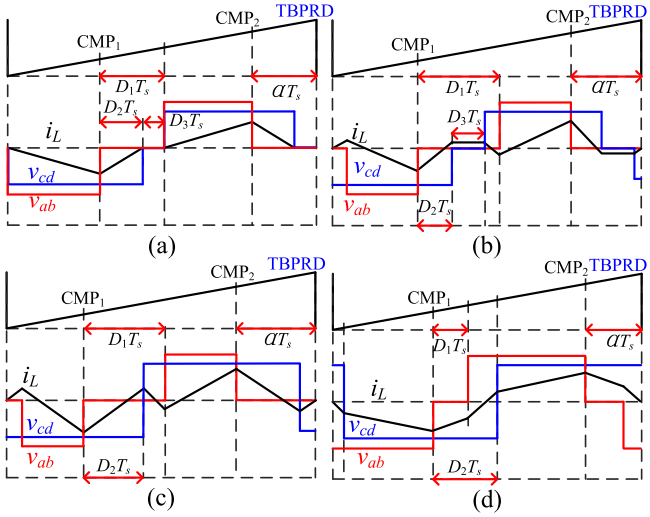

Fig. 6. Key waveforms of the four optimized modes with the ZCP based TPS modulation, (a) light load TPS-a, (b) light load TPS-b, (c) light load TPS-c, and (d) heavy load TPS-d.

current i_L is zero. The registers are updated here. Hence, the converter reaches its new steady-state instantly.

B. Analysis of ZCP Based VFM Modulation

VFM modulation for DAB is utilized in [15]–[17] to extend the ZVS range of the DAB converter. The proposed scheme can also be extended to VFM if the period register TBPRD is updated at the beginning of the new period as shown in Fig. 5. The scheme is similar to fixed-frequency modulation as analyzed in ZCP based SPS modulation.

C. Analysis of ZCP Based TPS Modulation

When k deviates from unity, DPS, EPS, and TPS modulations are more frequently employed. DPS and EPS are indeed the special cases of TPS. For buck mode in the forward direction, as analyzed in [8]–[14], the optimized scheme can be divided into two states: light load and heavy load. The light load and heavy load are defined as

$$\begin{cases} D_1 \geq D_2 + D_3, & Light\ load \\ D_1 < D_2 + D_3, & Heavy\ load. \end{cases} \tag{8}$$

Fig. 6 shows the key waveforms at the optimized steady state with α. There are three optimal control schemes for light load with TPS and EPS as shown in Fig. 6(a)–(c), and most of them

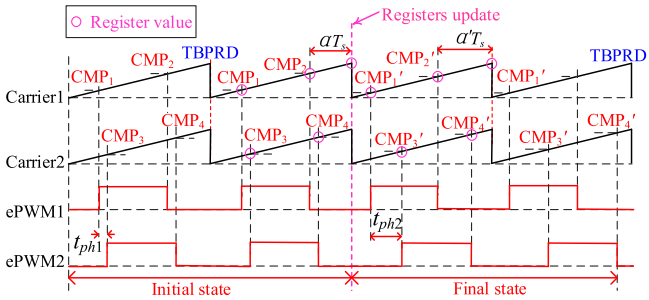

Fig. 7. Mechanism of switch pattern generation with the proposed method.

can achieve ZVS. Although Fig. 6(a) is non-ZVS state, the zero current state does not affect the phase shift ratio. Therefore, the effect of the ZVS condition can be ignored. It should be noted that there are multiple points, where the inductor current is zero at light load with TPS modulation. In order to combine different modes to get a unified expression, the second zero current point is adopted to determine α. At heavy load, the optimization algorithm tends to be EPS as shown in Fig. 6(d). Correspondingly, α can be derived similar to equations (3)– (5), the results are as follows:

$$\alpha = \begin{cases} \frac{k-1+2D_1+2D_3k+4D_2k}{4k}, & Light\ load \\ \frac{D_2k-\frac{1}{2}D_1+\frac{1}{4}(1-k)+D_1}{1+k}, & Heavy\ load. \end{cases} \tag{9}$$

The full model of DAB in the forward direction with the TPS modulation can be classed into six modes as analyzed in [12] and [13]. Here we do not analyze all of them in detail because the rest of them are seldomly used. The other cases can be analyzed similarly and the calculation results are identical. For instance, at heavy load, the calculation of (9) is the same as (6) when $D_1 = D_3 = 0$ in SPS. i_L is zero at the beginning and end of the carrier period in each mode. Then, seamless dynamic transition can be ensured when the registers are updated at the beginning of the following carrier period.

IV. Practical Design Considerations

A. Mechanism of Switch Pattern Generation

To produce the required driving signals, in the proposed controller, all the carriers are synchronized as shown in Fig. 7. The rising and falling edges of each leg (CMP_n, n=1,2,3...) are adjusted to generate the required phase shifts (D_1, D_2, D_3) and the additional variable α. For simplicity, only two driving signals (ePWM1, ePWM2) are described and the other signals can be analyzed similarly. The period register TBPRD is determined by the switching frequency. The distance between CMP_2 and TBPRD is synchronized by α. $CMP_{1(3)}$ and $CMP_{2(4)}$ are half a switching cycle apart to generate 50% duty cycle. The difference between CMP_3 and CMP_1 determines the phase shift between ePWM1 and ePWM2. It should be noted that CMP_n is compensated to be within the range of one period. As shown, when the phase shift between ePWM1 and ePWM2 changes from t_{ph1} to t_{ph2}, the registers are updated at the beginning of the following carrier period. Correspondingly, CMP_1-CMP_4

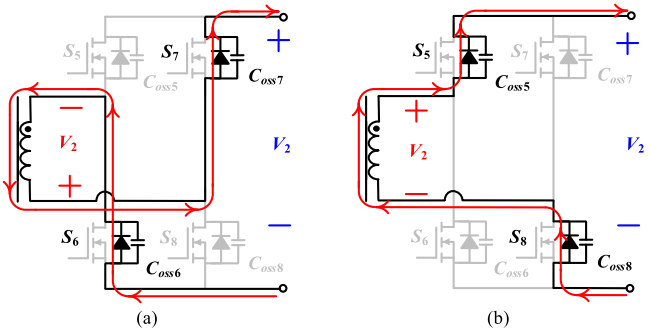

Fig. 8. Current path in the dead time before $S_{6,7}$ are turned on in (a) ZVS condition, (b) non-ZVS condition.

and α are updated to CMP$_1$′-CMP$_4$′ and α'. Then, the driving signals reach their new steady state.

B. Effect of the Dead Time in the SPS Modulation

When f_s is high, the effect of the dead time becomes apparent. The effect of the dead time in DAB is analyzed in [37]. In the SPS modulation, if the converter achieves ZVS as shown in Fig. 8(a), i_L is negative when $S_{5,8}$ are turned OFF. Then, the current freewheels through $S_{6,7}$. The stored energy in the junction capacitor $C_{oss6,7}$ is released to ensure ZVS. Therefore, v_{cd} decreases from positive to negative before $S_{6,7}$ are turned ON. However, when the converter loses ZVS completely, i_L is positive when $S_{5,8}$ are turned OFF as shown in Fig. 8(b). Then, the current freewheels through the parasitic diodes of $S_{5,8}$, and v_{cd} is still positive during the dead time until $S_{6,7}$ are turned ON. Therefore, in non-ZVS region, the dead time is added to the outer phase shift D_2T_s as

$$t_{ph\_non-ZVS} = D_2T_s + t_{dead} \tag{10}$$

where $t_{ph\_non-ZVS}$ and t_{dead} is the practical outer phase shift and dead time, respectively. Moreover, when the current polarity reverses during the dead time, the converter only achieves partial ZVS. The junction capacitors of the MOSFETs to be turned ON are first discharged and then charged if t_{dead} is sufficiently long. The profile voltage (v_{ab} or v_{cd}) reverses twice during the dead time [6]. This lead to the inaccurate of α. Practically, for high f_s, the dead time is usually designed to be fixed and sufficiently small for simplicity and better comprehensive performance. Moreover, the junction capacitance is highly nonlinear. Its value is typically more than ten times higher than the nominal value at low bias voltage. Thus, the small reverse current is unable to discharge the junction capacitance, and the profile voltage does not reverse during the dead time in the partial ZVS region.

Besides, it should be noted that at the beginning or end of each carrier period, v_{cd} is negative in non-ZVS region as shown in Fig. 4(a) and (c) and positive in the ZVS region as shown in Fig. 4(b), (d). When the converter operation changes from non-ZVS region to ZVS region [see Fig. 9(a)], the proposed method requires v_{cd} to have an additional rising edge at the beginning of the new period. Therefore, at the beginning of each carrier period in the ZVS region, there exists a falling edge in the gate signals of $S_{6,7}$ and a rising edge in the gate signals of

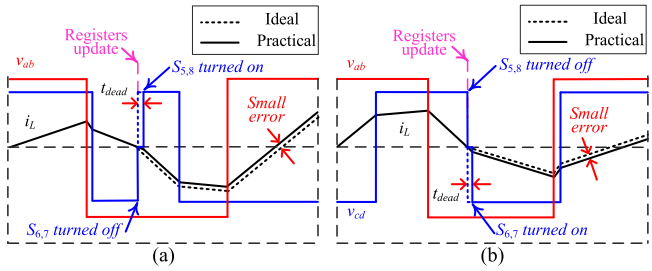

Fig. 9. Effect of dead time when the converter changes (a) from non-ZVS condition to ZVS condition, (b) from ZVS condition to non-ZVS condition, with SPS modulation.

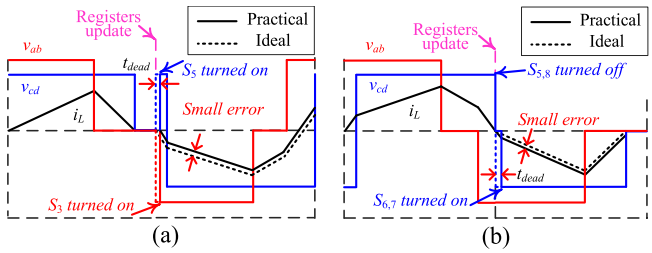

Fig. 10. Effect of the dead time when the converter changes (a) from non-ZVS condition to ZVS condition, (b) from ZVS condition to non-ZVS condition, with TPS modulation method.

$S_{5,8}$. Practically, $S_{6,7}$ are turned OFF instantly, v_{cd} rises from $-V_2$ to zero. However, there is a dead time before the turning ON of $S_{5,8}$. Hence, the rising edge of v_{cd} from zero to $+V_2$ is delayed by t_{dead}. Consequently, a small unbalanced volt-second nV_2t_{dead} occurs due to the dead time, and a small current error appears.

Similarly, as shown in Fig. 9(b), when the converter operation changes from ZVS region to non-ZVS region, the proposed method requires v_{cd} to have an additional falling edge at the beginning of the new period. Therefore, at the beginning of each carrier period in non-ZVS region, there exist a rising edge in the gate signals of $S_{6,7}$ and a falling edge in the gate signals of $S_{5,8}$. A small unbalanced volt-second $-nV_2t_{dead}$ occurs due to the dead time. Similar to the abovementioned case, this error is trivial and can be ignored with a sufficiently small dead time. Besides, the error only occurs when the state changes between non-ZVS region and ZVS region. Therefore, accurate transitions can be realized in most cases.

C. Effect of the Dead Time in TPS Modulation

Also, the nonideal dead time affects the transition between the light load region and the heavy load region in the TPS modulation. Taking the transition between (a) and (d) of Fig. 6 as an example. The details are depicted in Fig. 10. When the converter changes from TPS-a to TPS-d as shown in Fig. 10(a), $S_{3,5}$ are required to be turned ON at the beginning of the new period. However, due to the non-ideal dead time, an unbalanced volt-second, which is no larger than $(V_1 + nV_2)t_{dead}$ occurs. When the converter changes from TPS-d to TPS-a as shown in Fig. 10(b), the unbalanced volt-second equals $-nV_2t_{dead}$. Also, the appeared current error is very small and only occurs when

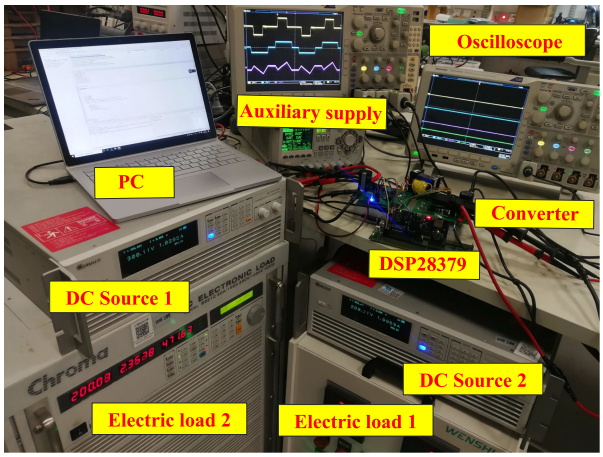

Fig. 11. Picture of the laboratory test bench.

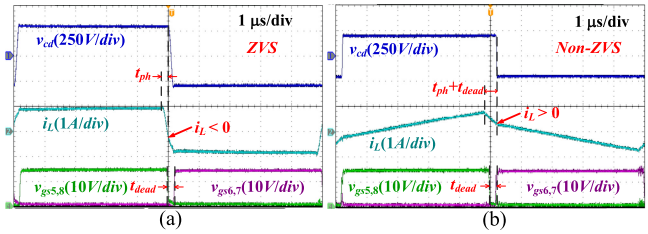

Fig. 12. Experimental waveforms of v_{cd} and i_L in (a) ZVS condition, (b) non-ZVS condition.

the state is changed between the light load and heavy load states. Therefore, it can be ignored if the dead time is sufficiently small.

D. Effect of the Potential Measurement Error

The proposed method fits to the applications with frequent power commutations between different energy sources. Besides, the converter operates with f_s much higher than the fluctuation frequency of the energy source voltage. Therefore, the port voltages V_1 and V_2 can be assumed to be constant over one switching period. Moreover, the calculation is related to the voltage conversion ratio k. Practically, there exist slight variations in the measured k. However, it is small enough under an acceptable level as analyzed in [31]. Therefore, the measured k can accurately predict the zero current point of the inductor.

V. Experimental Results

To verify the proposed concept, a DAB converter prototype to process the power flow between a 300 V port and a 200–280 V port is designed and tested. L is 86 μH; f_s is 100 kHz; t_{dead} is 100 ns; n is 30 : 30. The photo of the experimental setup is shown in Fig. 11. The two energy sources are emulated by two programmable power supplies (Chroma 62100H-450). The loads are emulated by two programmable electronic loads (Chroma 63212 and WS-LDZ20A-DC500 V). A DSP controller (TMS320F28379) from Texas Instruments is employed to realize the control algorithms.

Fig. 12 depicts the experimental waveforms of v_{cd} and inductor current i_L in ZVS and non-ZVS conditions. When the converter loses ZVS, the polarity reversal of v_{cd} occurs after the dead time as shown in Fig. 12(b). Then, the dead time is added to the practical phase shift. This agrees well with the analysis in Section IV-B. Fig. 13 shows the experimental waveforms of v_{ab} and i_L with partial ZVS and full ZVS when t_{dead} is 100 ns. As shown in Fig. 13(a), the current polarity reverses during the deadtime, which indicates a partial ZVS condition. v_{ab} does not reverse during the dead time until $S_{2,3}$ are turned ON. As shown in Fig. 13(b), the current polarity reverses after the deadtime, which indicates a full ZVS condition. v_{ab} reverse to negative before $S_{2,3}$ are turned ON, which means ZVS is achieved and a reasonable t_{dead} is selected. Also, this agrees with the analysis in Section IV-B.

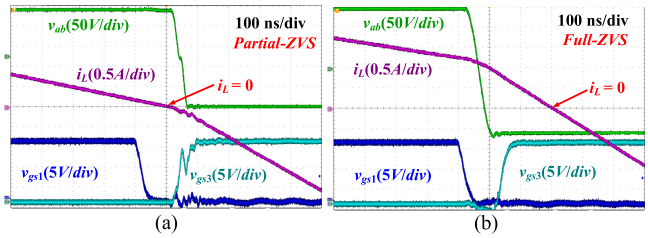

Fig. 13. Experimental waveforms of v_{ab} and i_L when (a) the current polarity reverse during the dead time and (b) the current polarity reverse after the dead time.

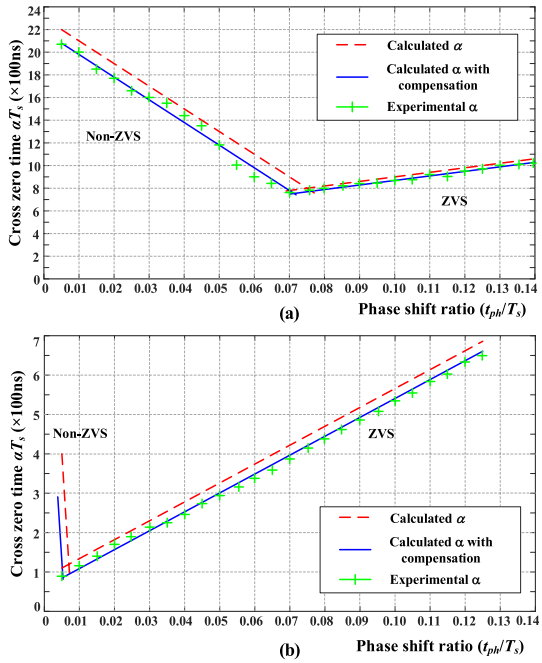

Fig. 14. Theoretical and experimental results of α when (a) $V_2 = 200\,V$, and (b) $V_2 = 280\,V$.

Fig. 14 shows the theoretical and experimental values of αT_s when V_2 is 200 V, 280 V, and f_s=100 kHz. The theoretical values are based on (6) and (10). The experimental values are the measured duration between the falling edge of v_{ab} and the zero current point of i_L. As shown, there is a minor error between the theoretical and experimental values due to the reason that the rising and falling edges of v_{ab} and v_{cd}, as well as the winding resistance, are not ideal in practice. Thus, compensation

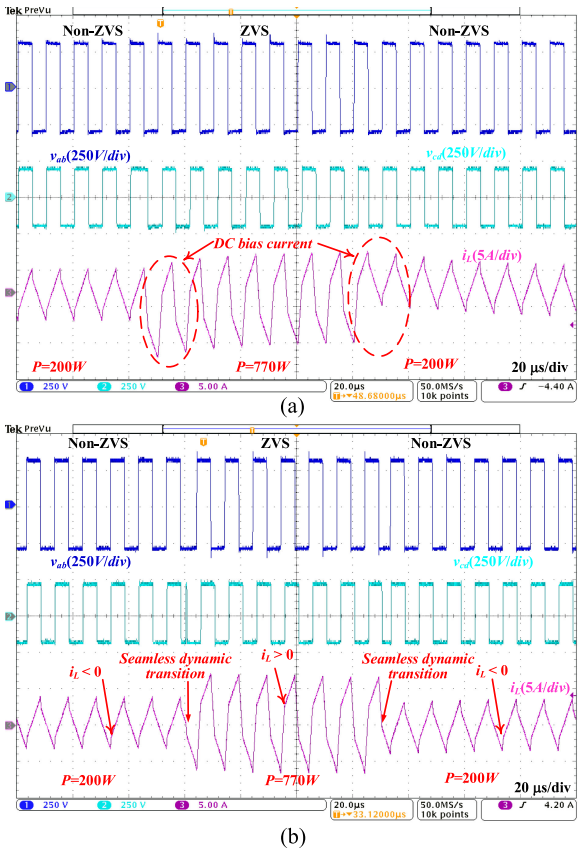

Fig. 15. Experimental waveforms with SPS modulation when the operation changes between non-ZVS region and ZVS region in the forward direction with (a) conventional method and (b) proposed method.

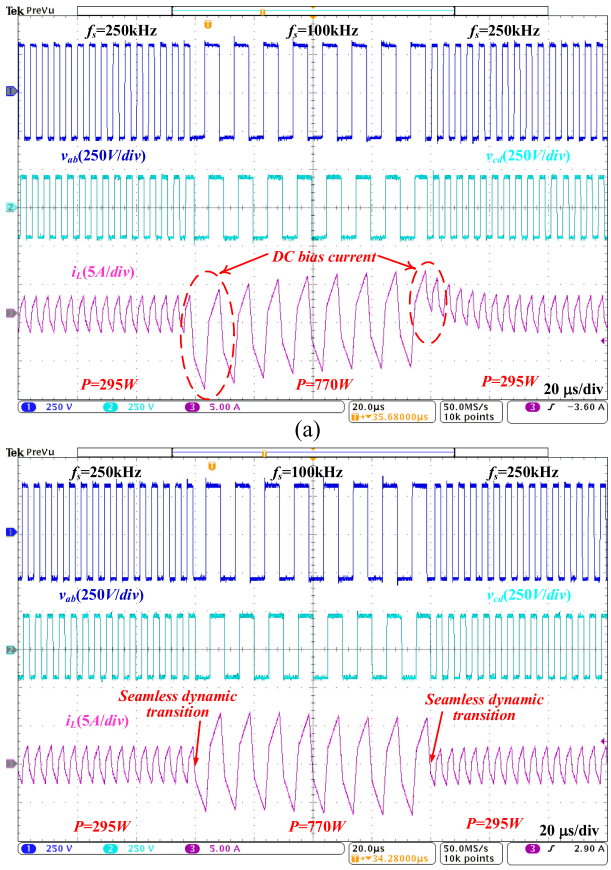

Fig. 16. Experimental waveforms in the forward mode with VFM modulation when load changes using (a) conventional method and (b) proposed method.

should be added to the calculated value. From the experimental results, the compensation is 20 ns in ZVS conditions and 100 ns in non-ZVS conditions. The compensated value agrees well with the experimental measurement, which secures a seamless dynamic transition.

Fig. 15 captures the experimental waveforms with the conventional modulation and the ZCP based SPS modulation in the forward mode when f_s is 100 kHz and V_2 is 200 V. This means k deviates away from unity. According to (7), ZVS is lost when D_2 is sufficiently small. The load first steps up from non-ZVS state to ZVS state and then steps down to non-ZVS state. The transferred power changes from 200 to 770 W and then back to 200 W. As shown in Fig. 15(a), i_L has a dc bias current during both the transient intervals with conventional modulation. The dc bias current can be damped by the winding resistance. The soft-switching performance gets worse during the transient interval, which leads to additional stress on the power devices. However, with the proposed method as shown in Fig. 15(b), the dynamic response is instantly achieved without dc bias current and transient issues. There is a minor error in i_L as analyzed in Section IV-B. This error is trivial and can be ignored. The results validate that the proposed control scheme is effective under ZVS, non-ZVS regions.

Fig. 16 captures the experimental waveforms with the conventional modulation and with the ZCP based VFM modulation in the forward mode when V_2 is 200 V. VFM modulation can increase D_2 in light load and extend the ZVS range with a higher f_s. The load first steps up from 295 to 770 W and then back to 295 W, f_s changes from 250 to 100 kHz and then back to 250 kHz. As shown in Fig. 16(a), dc bias current appears with the conventional modulation. The ZVS is lost during the transition. However, with the proposed method as shown in Fig. 16(b), the dynamic response is instantly achieved without transient issues. It can be noted that there is a small decreasing trend during the transient process. This is because the mismatch of loop resistances incurs a trivial steady-state dc bias current. The system needs to reestablish the steady-state dc bias current. The results validate that the proposed control scheme is effective with the VFM modulation.

Fig. 17 shows the experimental waveforms with ZCP based SPS modulation when the power flow direction changes. V_2 is 280 V and f_s is 100 kHz. A sequence of power references is set to be 350 W, 930 W, −930 W, −530 W, 350 W to evaluate the dynamic response performance. The experimental waveforms indicate that the proposed method is effective in bidirectional power transmission, the dynamic response is instantly achieved without dc bias current and transient issues. Besides, the transient ZVS can be achieved as analyzed in [31].

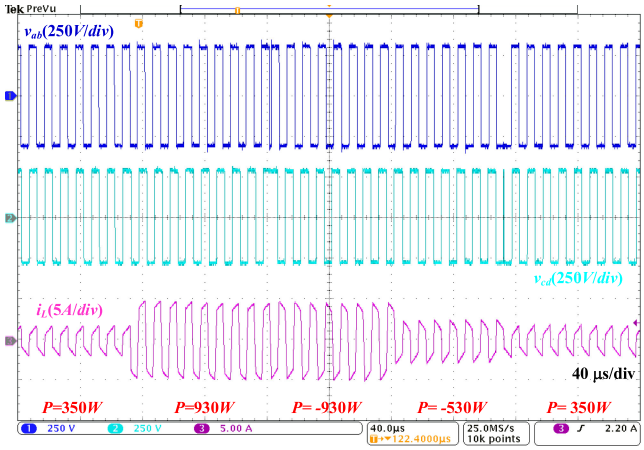

Fig. 17. Experimental waveforms with SPS modulation when the power flow direction changes.

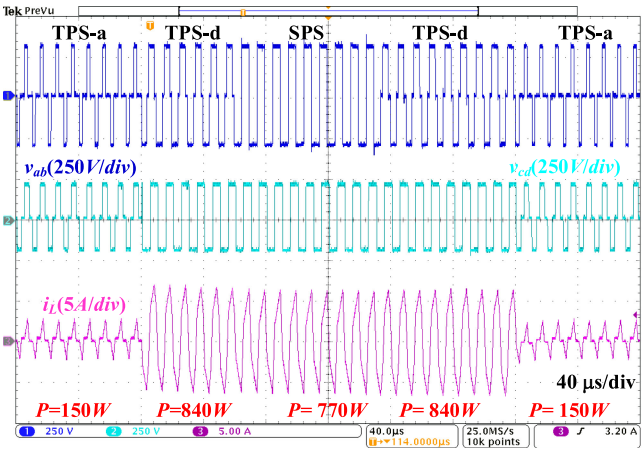

Fig. 18. Experimental waveforms in the forward mode when the modulation method changes.

Moreover, to verify the feasibility of the proposed scheme in the TPS modulation, the proposed control scheme is also tested in TPS. As shown in Fig. 18, the modulation method changes following the sequence of TPS-a, TPS-d, SPS, TPS-d, TPS-a when V_2 is 200 V and f_s is 100 kHz. Fig. 19 depicts the modulation method changes following the sequence of TPS-b, TPS-d, TPS-c when V_2 is 200 V and f_s is 100 kHz. The experimental results disclose that the proposed method is effective in TPS and can realize smooth transition between different modulation methods. Also, there is a minor error in i_L as analyzed in Section IV-C when the converter changes between the light load region and heavy load region. This error is trivial and can be ignored. Moreover, due to the constant unbalanced volt-second caused by the dead time, this error is independent of the load power. The proposed method can also be applied to other modes of TPS. It is similar to the abovementioned modes.

VI. Conclusion

In this article, a novel digital control scheme was proposed for DAB converters. It was based on zero current prediction

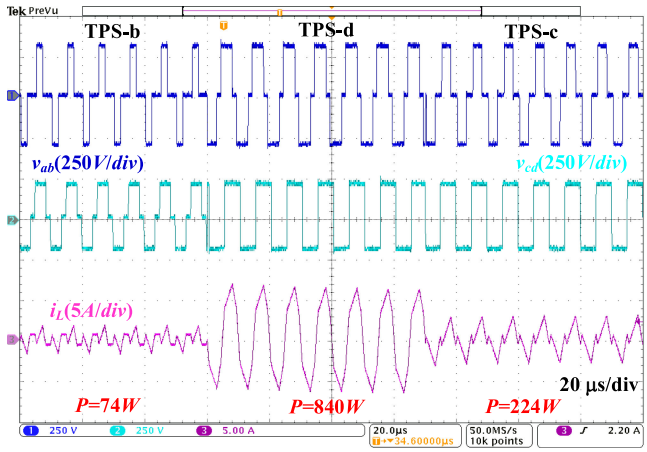

Fig. 19. Experimental waveforms in the forward mode with TPS when the load changes.

and can achieve a seamless dynamic transition with zero dc bias current. Compared with the traditional methods, only an additional variable was introduced to ensure i_L equals zero at the end of the carrier period. The calculation was simple and the implementation was easy. The extra control variable was only determined by k and the phase shifts between L_1–L_4, and was insensitive to the converter parameters.

A comprehensive set of experiments were conducted to validate the advantages of the proposed ZCP based control scheme. The proposed control scheme was proved to be effective when the load changes in ZVS, non-ZVS regions, unidirectionally, bidirectionally, even when the modulation method and switch frequency changes. Although the transitions between ZVS and non-ZVS regions were accompanied by small error, the error was trivial since the dead time was really small. The experimental results exhibit excellent dynamic response performance. Both the transient issues and the dc bias current, which exist using the conventional control scheme, were eliminated.

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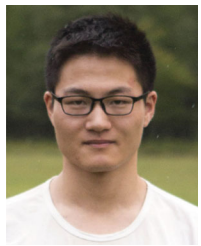

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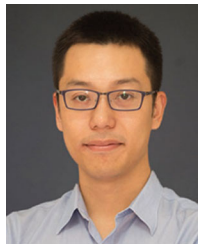

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