Hierarchical Modular Battery Equalizer With Open-Loop Control and Mitigated Recovery Effect

Faxiang PENG, Yiqing LU, Mingde ZHOU, and Haoyu WANG

***Abstract*—In this manuscript, an advanced battery equalizer with open-loop control is proposed. This equalizer is based on a two-layer hierarchical modular architecture. The top string-to-module (S2M) layer consists of a half-bridge inverter and a voltage multiplier (VM) rectifier, and the bottom cell-to-cell (C2C) layer is implemented by bidirectional buck-boost units. Without state-of-charge (SOC) estimation, the battery charge can be automatically transferred from high-voltage cell-modules/cells to low-voltage ones. Only a pair of symmetrical pulse width modulation (PWM) driving signals with fixed switching frequency and duty cycle are required.This reduces the control complexity remarkably. Meanwhile, the balancing current of each balancing path naturally attenuates with the convergence of cell-module/cell voltages. This ensures a fast balancing of cell-module/cell with large voltage mismatch. The battery-recovery-effect induced balancing error is also effectively mitigated. Moreover, simple control facilitates a simultaneous module and cell voltage balancing in static, charging, and discharging conditions. The operation principles are analyzed in detail. An experimental platform with eight series-connected batteries is built and tested. The measured results well validate the theoretical analysis. Both cell and module voltages automatically converge with clearly mitigated recovery effect.**

***Index Terms*—Battery equalizer, battery recovery effect, current-converge, open-loop control.**

I. Introduction

In high power energy storage systems, the low-voltage lithium batteries are typically connected in series to meet the high voltage and power requirements [1], [2]. In battery strings, the cell mismatch issues occur due to the manufacturing and environmental variation. Certain cells may be overcharged or discharged, which limits the lifetime and available battery capacity, and even incurs hazards such as fire/explosion [2].

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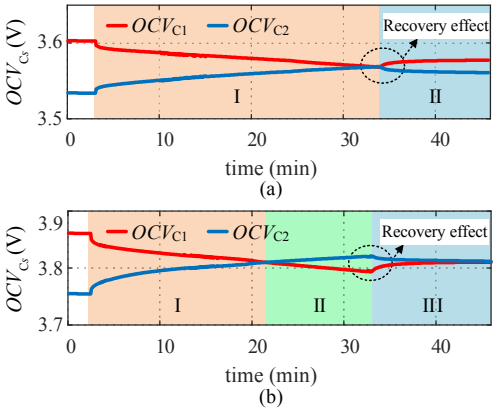


Fig. 1. Open circuit voltages with different equalization stages. (a) Without recovery-eliminating stage and (b) with recovery-eliminating stage.

Thus, battery balancing techniques are necessary to mitigate this mismatch and to extend the battery lifetime.

Among the reported battery balancing methods, the control complexity, equalization accuracy, balancing speed, circuit extendibility, and conversion efficiency are the main criteria to evaluate the balancing performance. Traditional shunting resistor based passive equalizers are widely utilized due to its low cost and simplicity [1]. However, they suffer from zero efficiency and heat management issues. Thus, many high-efficiency power electronic equalizers are developed and evaluated, such as buck-boost converters [3]–[6], switched capacitor converters [7]–[12], multi-winding transformer converters [13]–[18], and voltage multiplier (VM) [19]–[22]. These active balancing methods can be divided into two categories: 1) constant-current balancing [3], [4] and 2) current-converge balancing [5]–[22], according to the characteristics of balancing current during the balancing process.

In [3], a buck-boost based hierarchical equalizer is controlled to achieve constant-current balancing. It provides a programmable balancing current for every unbalanced cell/string pair. However, it's hard to be deployed in long battery string scenarios. To improve the extendibility, a hybrid hierarchical equalizer which combines LLC based module equalizer and buck-boost based cell equalizer is introduced in [4]. However, it is also flawed with complex control. Moreover, both constant-current balancing methods suffer from battery recovery effect which causes a clear voltage departure after voltage convergence as shown in Fig. 1(a). To mitigate this error, a recov-

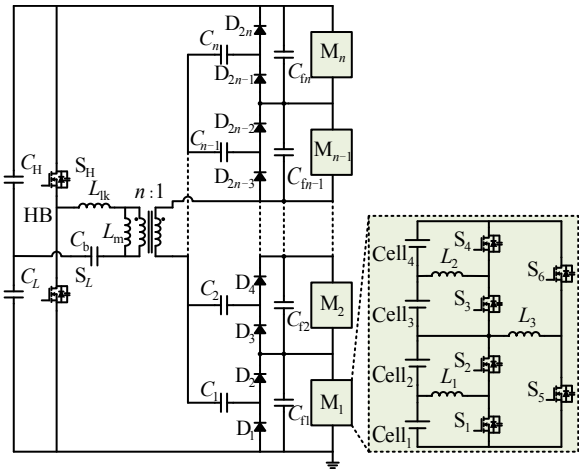


Fig. 2. Schematic of the proposed modular equalizer with *n* cell modules.

ery-eliminating stage (see stage A in Fig. 1(b)) based on state-of-charge (SOC) estimation is needed, which further increases the control complexity.

Some current-converge balancing techniques are proposed. In these methods, current flows naturally from the high-voltage cell to the low-voltage cell. Although the balancing speed is limited near finishing point because of small voltage differences between battery cells, the method exhibits advantages in mitigated recovery effect and low control complexity. In [5] and [6], bidirectional buck-boost based equalizers with multi-phase/coupled structure are investigated to mitigate cell voltage mismatch. To improve the balancing speed, some methods to increase the number of balancing paths or to decrease the average balancing path are proposed, such as double-tiered switched capacitor method [12], chain-structured method [8], and coupling all energy transfer capacitor [9]. However, the turning off loss at high frequency is problematic due to high balancing current.

To improve the conversion efficiency, several methods are proposed. In [11], a resonant mode is utilized in switched capacitor based equalizer to achieve zero-current switching. Meanwhile, in this method, the balancing current can be decided by parasitic and cell voltage difference when switching frequency is fixed [10]. This means the control complexity can also be reduced.

Except for the optimized switched capacitor method, multi-winding transformer based solutions [13]–[18] are also emerging. These solutions supress switching loss by decreasing the number of switches. However, they suffer from bulky circuit size because of the magnetic components. The coupled half-bridge structure [13], [14] and the flyback-forward operation integrated methodology [18] are developed to reduce the number of transformers/windings, but the mismatch of leakage inductance causes transient issues. Despite this, the decreasing number of switches makes it much simpler to control.

To further improve the control complexity, in [19]–[22], VM is utilized to achieve an automatic voltage balancing. This reduces the number of active components and driving signals, which facilitates a low circuit profile. However, the introduction of passive components and diodes causes more conversion loss.

In this manuscript, a hierarchical modular battery equalizer with open-loop control and current-converge balancing is proposed. Fig. 2 shows the schematic of the proposed equalizer. As shown, the battery string is configured into multiple cell modules with modular equalizer. The string-to-module (S2M) equalizer combines a half-bridge inverter and a VM rectifier. The cell-to-cell (C2C) equalizer consists of buck-boost converter. The proposed equalizer has following advantages: 1) Fast balancing speed: both module and cell balancing operate simultaneously in static, charging, and discharging conditions. 2) Simple control: only a pair of pulse width modulation (PWM) driving signals with fixed f_s and D are required for each half-bridge. 3) Mitigated recovery effect: the balancing currents naturally attenuate as the cell-module/cell voltages converge. This ensures an effective mitigation of battery recovery effect. Hence, the overall control complexity is reduced significantly and it is easier to deploy into long battery string scenarios.

II. Operation Principles

A. Hierarchical Equalization Structure

As shown in Fig. 2, this modular equalizer combines a half-bridge inverter and a VM rectifier in the S2M layer. The C2C layer is based on a two-layer buck-boost architecture. This hierarchical structure provides more available balancing paths of unbalanced modules/cells [3], [13], [20]. Typically, in S2M layer, each balancing path of battery module is established by the passive components (energy transfer capacitors (C_1–C_n) and rectifier diodes (D_1 – D_{2n})) instead of the multiplex network requiring numerous active switches [4], ensuring a compact circuit size. The input port of the half-bridge inverter is paralleled with the battery string, and the output ac square wave is rectified by the VM rectifier. When the VM rectifier enters into the steady state, the voltage (VC_{fi}) across each filtering capacitor (C_{f1}–C_{fn}) is equal. Thus, the charge of the battery string can be transferred to each module in this circulating way, and module voltages are balanced automatically. On the other hand, in each battery module with four cells, the bidirectional buck-boost converter with two parallel layers is utilized to transfer charge between two cells/strings.

In the proposed structure, automatic balancing with open-loop control is utilized. In the S2M layer, the MOSFETs of half bridge work symmetrically at fixed f_s and D. In the C2C layer, symmetric PWM signals with fixed f_s and D are applied to MOSFETs of each equalizer unit. The PWM signals can be shared if both layers work at the same frequency, thus a low control complexity is achieved.

B. Module Equalizer

Since the proposed module and cell equalizer is configured at different balancing layer, they can be controlled and ana-

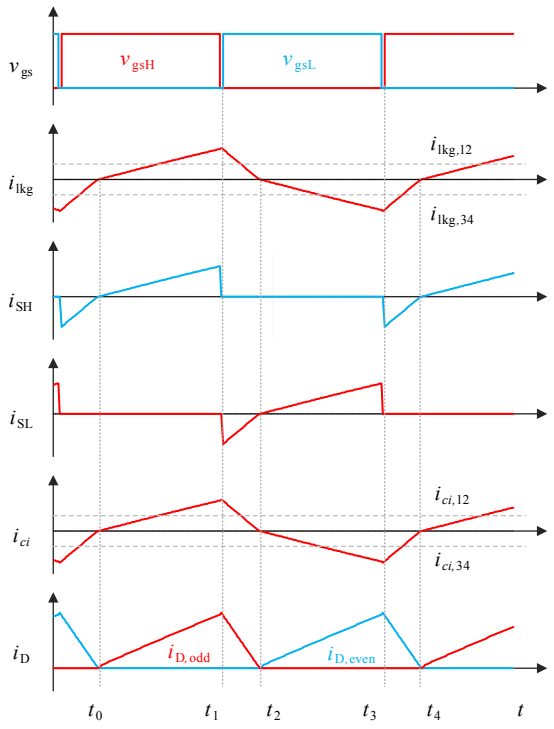


Fig. 3. Key waveforms of the module equalizer.

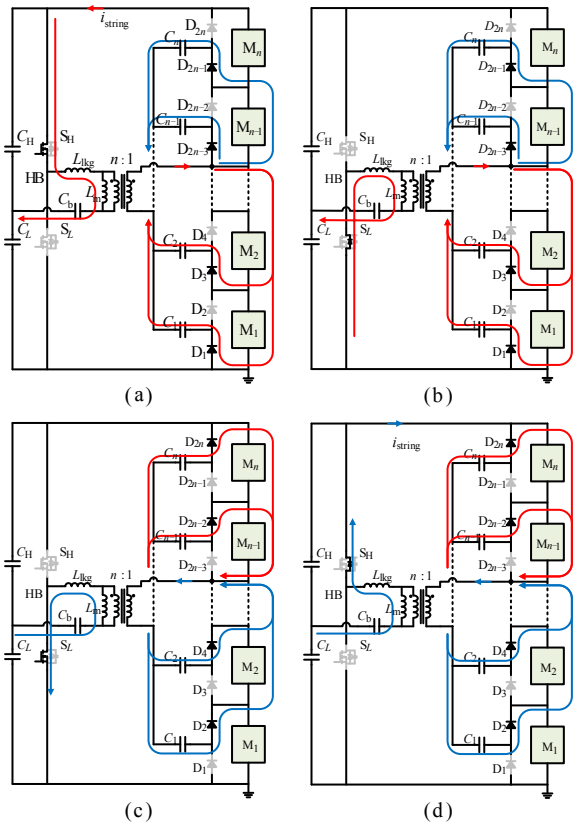


Fig. 4. Current flow paths of the module equalizer. (a) Mode 1, (b) mode 2, (c) mode 3 and (d) mode 4.

lyzed separately. This subsection focuses on the analysis of the operation for the half-bridge and VM rectifier based module equalizer. Fig. 3 shows the key waveforms of the module equalizer, the primary half-bridge MOSFETs turn on and off symmetrically with certain dead time. f_s and D of PWM signals are fixed. Correspondingly, the current flow path of the module equalizer for n-cell modules are shown in Fig. 4. To simplify the analysis, the filtering capacitor of each circuit unit in VM rectifier is ignored since it doesn't affect the steady state operation.

As shown in Fig. 4, one switching period could be divided into four operation modes. Assuming the capacitance of c_i is small enough, the voltage variations of c_i have less impact on the cell module (M_i). Therefore, the voltage variations of M_i (ΔV_{Mi}) can be ignored compared to the voltage variations of c_i (ΔV_{ci}) at the time scale of the switching period. Thus, the cell module can be seen as a constant voltage source. Meanwhile, the charge-transfer feature of VM rectifier is similar to the switched capacitor converters [23] and its detailed analysis has been presented in [24]. Thus, this analysis of VM rectifier based module equalizer is also similar to switched capacitor converter, which models c_i as a resistive component.

During the charge transportation process, the leakage inductor (L_{lkg}) of the transformer is charged and discharged as the half-bridge MOSFETs turn on and off. Typically, Fig. 4 (a) and (b) shows the first two operation modes (modes 1 & 2), i_{lkg} linearly increases and then decreases to zero as shown in Fig. 3. The current of c_i (i_{ci}) shows similar feature as the odd-numbered diodes $D_{i,\,odd}$ conduct, and c_i is charged. Within these two modes, by considering the resistance of c_i (r_{ci}) and D_i (r_{Di}) the average secondary voltage of transformer V_{S12} can be derived as,

$$\begin{aligned} V_{S12} &= V_S \\ &= V_{c1,\,peak} + V_{D1} + I_{c1,12}(r_{c1} + r_{D1}) + V_{M\frac{n}{2}} \\ &\quad + V_{M\frac{n}{2}-1} + \cdots + V_{M_2} + V_{M_1} \\ &= \vdots \\ &= V_{c\frac{n}{2}+1,\,peak} + V_{D_{n+1}} + I_{c\frac{n}{2}+1,12}(r_{c\frac{n}{2}+1} + r_{D_{n+1}}) \\ &= \vdots \\ &= V_{cn,\,peak} + V_{D_{2n-1}} + I_{cn,12}(r_{cn} + r_{D_{2n-1}}) \\ &\quad - V_{M\frac{n}{2}+1} - \cdots - V_{M_{n-2}} - V_{M_{n-1}} \end{aligned} \tag{1}$$

where $V_{ci,\,peak}$ and $I_{ci,12}$ are the average values of v_{ci} and i_{ci} respectively, within modes 1 and 2. V_{Di} is the forward voltage drop of D_i, V_{Mi} is the terminal voltage of cell module. Meanwhile, the average of i_{lkg} is,

$$I_{lkg,12} \cdot n = I_S = \sum I_{ci,12} = I_{c1,12} + I_{c2,12} + \cdots + I_{cn,12} \tag{2}$$

In Fig. 3, as i_{lkg} continues to fall to its negative value during modes 3 and 4, i_{ci} follows this pattern due to the even-numbered diodes $D_{i,even}$ conduct as shown in Fig. 4 (c) and (d). In these two modes, V_{S34} can be derived as:

$$\begin{aligned} V_{S34} &= -V_S \\ &= V_{c1,\text{valley}} - V_{D2} - I_{c1,34}(r_{c1} + r_{D2}) + V_{M\frac{n}{2}} \\ &\quad + V_{M\frac{n}{2}-1} + \cdots + V_{M3} + V_{M2} \\ &= \vdots \\ &= V_{c\frac{n}{2},\text{valley}} - V_{Dn} - I_{c\frac{n}{2},34}(r_{c\frac{n}{2}} + r_{Dn}) \\ &= \vdots \\ &= V_{cn,\text{valley}} - V_{D2n} - I_{cn,34}(r_{cn} + r_{D2n}) - V_{M\frac{n}{2}+1} \\ &\quad - \cdots - V_{Mn-1} - V_{Mn} \end{aligned} \tag{3}$$

where, $V_{ci,\text{valley}}$ and $I_{ci,34}$ are the average values of v_{ci} and i_{ci} respectively, within modes 3 and 4. The corresponding average of i_{lkg} is

$$I_{\text{lkg},34} \cdot n = I_S = \sum I_{ci,34} = I_{c1,34} + I_{c2,34} + \cdots + I_{cn,34} \tag{4}$$

In one switching period, the current path of cell module balancing can be established depending on the charging/discharging of c_i. At steady state, c_i maintains its charge-balance. Thus,

$$I_{c1,12}(t_2 - t_0) = I_{c1,34}(t_4 - t_2) \tag{5}$$

The duty cycle of symmetrical PWM signal should be set as 0.5 (i.e., $t_2 - t_0 = t_4 - t_2$) to ensure the average winding voltage of transformer equals zero. The parameter variation between each c_i and D_i can be ignored. Thus, combining (1)–(5), it can be derived that,

$$\Delta V_{ci} = 2V_S - 2V_D - 2I_c(r_c + r_D) - V_{Mi} \tag{6}$$

According to the variation of capacitor charge in on switching period (T_s), ΔV_{ci} can be derived as:

$$\Delta V_{ci} = \frac{I_{ci} T_s}{C_i} = \frac{I_{ci}}{C_i f_s} \tag{7}$$

where C_i is the capacitance of c_i, and f_s is the switching frequency. Combining (6) and (7), we have

$$I_{ci}\left[2(r_c + r_D) + \frac{1}{C_i f_s}\right] = 2V_S - 2V_D - V_{Mi} \tag{8}$$

Since the unit of $1/C_i f_s$ is Ω, the left side of (8) can be defined as:

$$R_{eqi} = 2(r_c + r_D) + \frac{1}{C_i f_s} \tag{9}$$

Following Kirchhoff current law (KCL) and Kirchhoff voltage law (KVL), an equivalent circuit for n-cell modules shown in Fig. 5 can be built according to (8) and (9). As shown, each module receives charge via two diodes and one R_{eqi}, and its balancing path is paralleled with a common voltage source ($2V_S$). The secondary current I_S distributes to M_i, and a larger

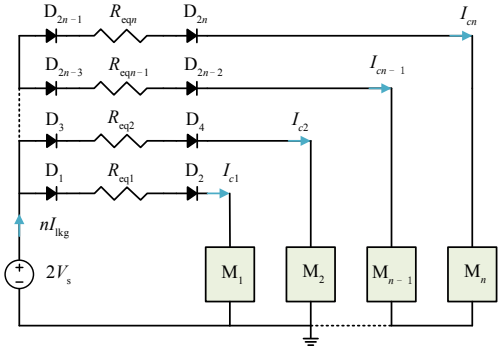


Fig. 5. DC equivalent circuit of the module equalizer.

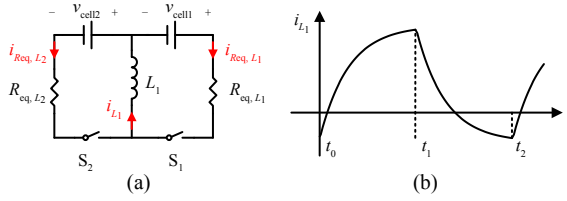


Fig. 6. Cell equalizer with (a) $R_{eq,Li}$ and (b) inductor current waveform.

balancing current I_{ci} can be achieved automatically for modules with lower V_{Mi}. This achieves an automatic and efficient module balancing, and ensures a fast charge compensation for low-voltage modules without SOC estimation based complex control algorithm. Each I_{ci} drops along with the increase of V_{Mi}. Meanwhile, the variation of each R_{eqi} may cause some mismatch of V_{Mi}, and a high R_{eqi} may lead to high conduction loss (i.e., $I_{ci}^2 R_{eqi}$). Meanwhile, the variation of R_{eqi} and V_{Di} may cause some mismatch of V_{Mi}. Based on (9), to mitigate the mismatch, diodes with low forward voltage drop and capacitors with high capacitance should be selected. Moreover, the S2M layer should be designed to work at a high f_s to further reduce R_{eqi}.

As mentioned before, the voltage of the string is applied to the half-bridge inverter. The charge of string is delivered via VM rectifier to balance each module. All modules can be balanced simultaneously by applying this power-circulating technique.

C. Cell Equalizer

The automatic equalization current depends on the voltage difference. Since the voltage difference between cells degrades during the balancing process, the loop resistance of buck-boost unit becomes critical to restrict balancing current near equalization finish point. This manuscript introduces the analysis of the cell equalizer considering the loop resistance ($R_{eq,Li}$), as shown in Fig. 6 (a). The inductor current is illustrated in Fig. 6 (b) when $R_{eq,Li}$ is significant.

a) S_1 turns on at $t = t_0$: Assume that $v_{Cell1}(t)$ changes little in one switching period, i.e., $v_{Cell1}(t) \equiv v_{Cell1}(t_0)$ for $t_0 \leqslant t \leqslant t_2$. Thus,

$$L_1 \frac{di_{L_1}}{dt} = v_{\text{Cell},1}(t) - R_{eq,L_1} i_{L_1}(t) \tag{10}$$

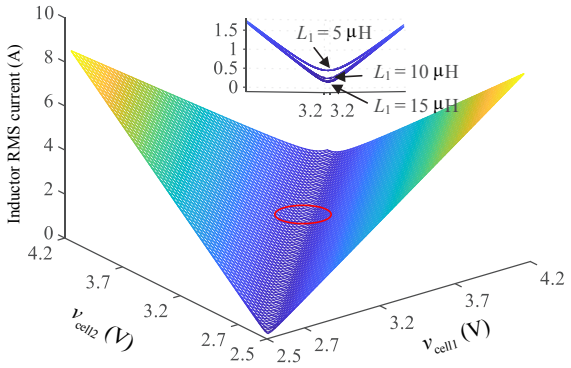


Fig. 7. Cell RMS current with different L_1 at $R_{eq,L} = 100$ mΩ.

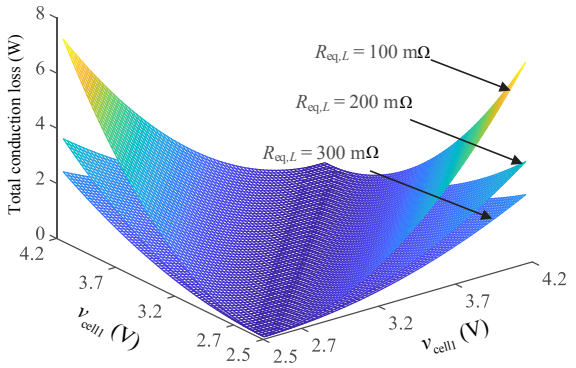


Fig. 8. Total conduction loss with different $R_{eq,L}$ at $L_1 = 10$ μH.

where R_{eq,L_1} is the loop resistance when S_1 is turned on.

b) S_2 turns on and S_1 turns off at $t = t_1$: In the deadband, the inductor current $i_L(t_1^-)$ and $i_L(t_1^+)$ is continuous considering MOSFETs commutation. Mark R_{eq,L_2} as the loop resistance when S_2 is on. The deadband is ignored as it occupies a small-portion of the period. Similar to (10), after $t = t_1$,

$$L_1 \frac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = -v_{\mathrm{Cell},2}(t) - R_{\mathrm{eq},L_2} i_{L_1}(t) \tag{11}$$

(10) and (11) show that $R_{eq,Li}|_{i=1,2}$ determines the slope of the inductor current i_{L1}. The total root-mean-square (RMS) current during one switching period is,

$$i_{L_1,\mathrm{RMS}} = \sqrt{\left[\frac{1}{T_s}\int_{t_0}^{t_1} i_{L1}^2(t)\mathrm{d}t + \int_{t_1}^{t_2} i_{L1}^2(t)\mathrm{d}t\right]} \tag{12}$$

To provide an even equalization process, the circuit layout should be symmetrical, i.e., $R_{eq,L_1} = R_{eq,L_2} = R_{eq,L}$. By applying a symmetrical PWM signal with 50% duty cycle and 200 kHz switching frequency, the total RMS current and conduction loss can be calculated, and are depicted in Figs. 7 and 8. These figures reveal that the variation of inductance doesn't show an obvious effect on RMS inductor current. Moreover, a larger loop resistance offers a smaller total conduction loss.

Near equalization region (i.e., $v_{\mathrm{Cell},1} \approx v_{\mathrm{Cell},2}$), the balancing current will converge to zero due to the small voltage differences between cells. Therefore, the loss and voltage drop on the loop resistance will also converge to zero. Meanwhile, the recovery effect can be mitigated because of small balancing current near the finishing point.

III. Experimental Verification

A. Experiment Setup

To evaluate the balancing performance of the proposed equalizer, a laboratory prototype to balance eight series-connected cells is built and tested. Figs. 9 and 10 show the schematic and photo

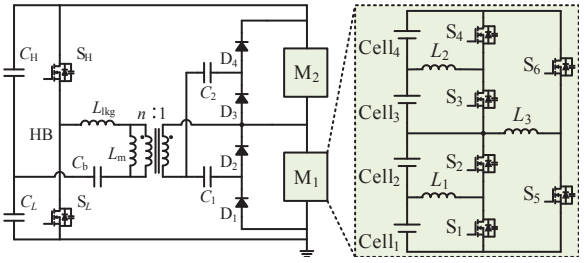
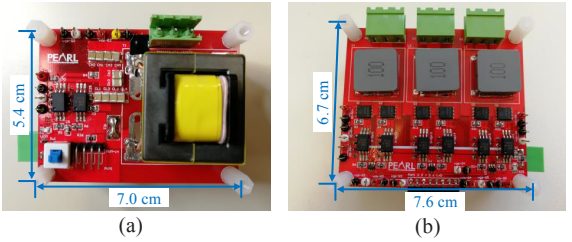


Fig. 9. Schematic of the experimental prototype.



(a) (b)

Fig. 10. Photos of the experimental prototype. (a) Module equalizer and (b) cell equalizer.

of the experimental prototype. Table I lists its main parameters. NCR18650PF Lithium-ion cells are employed to build the battery string. To ensure a high conversion efficiency, Schottky diodes (STPS5L60S) with low forward voltage and energy transfer capacitor with large capacitance (i.e., 47 μF) are selected. Moreover, a monitor IC (BQ76PL536) is utilized to detect cell voltages without the requirement of numerous isolated voltage sensors. As shown in Figs. 9 and 10, every equalizing unit is symmetrical, cell and module equalizer can be designed and controlled separately thanks to the modular structure. This simplifies its control and facilitates its adoption in large-scale energy storage systems.

B. Experiment Results

1) Key Waveforms

Figs. 11 and 12 show the steady-state switching waveforms

TABLE I
MAIN PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Module equalizer (half-bridge and VM)	MOSFETs	BSC093N04LS
	Magnetizing inductor	L_m : 130 μH
	Leakage inductor	L_{lkg} : 8.2 μH
	DC blocking capacitor	C_{bk} : 200 μF
	Switching frequency	200 kHz
	Energy transfer capacitor	C_i : 47 μF
	Diodes	STPS5L60S
	Turns ratio	1 : 1
Cell equalizer (buck-boost)	MOSFETs	BSC050NE2LS
	Inductors	L_1 : 10 μH
		L_2 : 10 μH
		L_3 : 15 μH
	Switching frequency	200 kHz
	Monitor IC	BQ76PL536
	Controller	TMS320F28379
	Battery	NCR18650PF

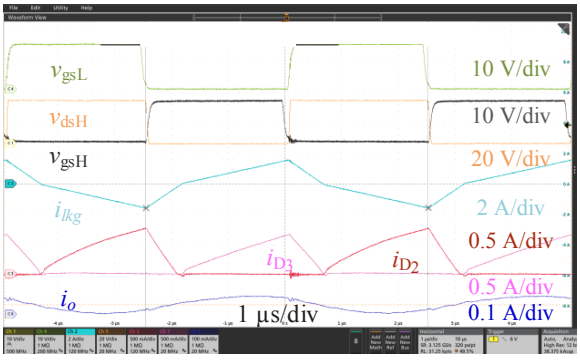


Fig. 11. Key waveforms of the module equalizer.

of module and cell equalizer during the balancing process, respectively. In Fig. 11, the high-side MOSFET v_{dsH} shows a smooth transition without voltage overshoot. The rectifier diodes conduct alternatively along with the leakage current i_{lkg} and the symmetrical V_{gs} signals, which validates the theoretical analysis in Fig. 3. Moreover, the key operation state in Fig. 12 indicates that MOSFETs realize zero-voltage-switching (ZVS) turn on and the currents of inductors (i_{L_1}, i_{L_2}, i_{L_3}) linearly increase and decrease to balance the adjacent cell/string pair.

2) Measured Efficiency

In order to evaluate the conversion efficiency, the measured efficiency data is captured and plotted in Figs. 13 and 14 (a). For the bidirectional buck-boost based cell equalizer, in Fig. 13, each layer exhibits a peak efficiency of 92.83% and 93.82%, respectively. It should be noted that the portion of conduction loss versus the total power loss increases significantly during the low-power region, leading to a sharply efficiency degradation. Correspondingly, in Fig. 15, the output currents of two balancing layers attenuate as the voltage difference of two unbalanced cells/cell-strings converges. Clearly, both currents attenuate close to zero near the balanced region (small voltage difference) in the same manner shown in Fig. 7.

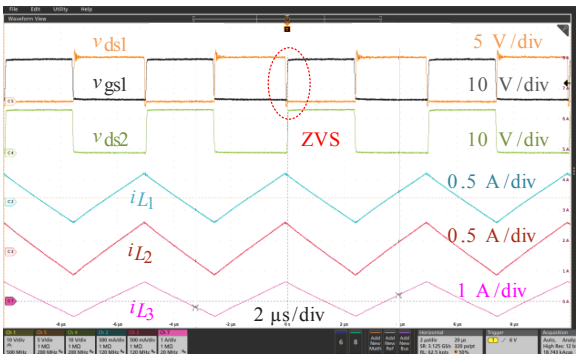


Fig. 12. Key waveforms of the cell equalizer.

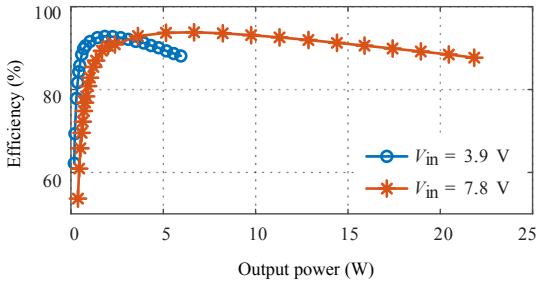


Fig. 13. Measured efficiency of the cell equalizer.

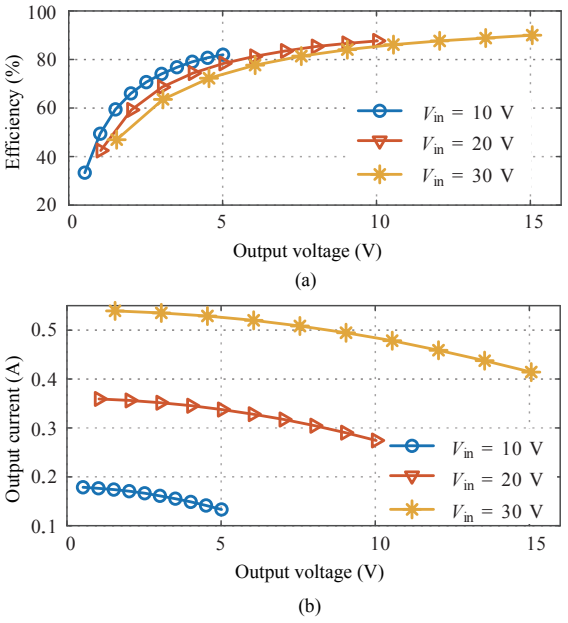


Fig. 14. Module equalizer. (a) Measured efficiency and (b) output Current.

Fig. 16 depicts the schematic of the module equalizer for efficiency measurement, which utilizes a DC power source (V_{in}) and a variable load (R_{var}) to easily establish the operation process from unbalanced to balanced. As shown in Fig. 14 (a), for a fixed V_{in}, the measured efficiency increases as the output voltage (V_{cf1}) increases due to the portion of the forward voltage drop of diode versus V_{cf1} decreases. This means VM based equalizer is more suitable for cell module balancing (high output

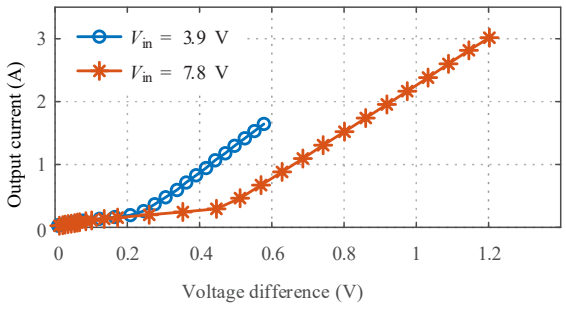


Fig. 15. Output current versus voltage difference for cell equalizer.

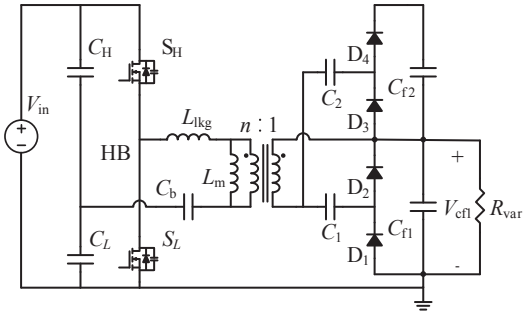


Fig. 16. Schematic of the module equalizer for efficiency measurement.

voltages). Fig. 14 (b) shows that low voltage corresponds to high output current, achieving a fast balancing performance of low-voltage module.

3) Voltage of Cells and Modules

Fig. 17 plots the cell and module voltages of eight series connected cells with initial voltage mismatch (i.e., V_{CT1}–V_{CT8} = (3.064, 3.557, 3.606, 3.6976, 3.556, 3.6886, 3.7556 and 3.834 V)) when the cell string is in static condition. After the balancing process of 223 min, both cell and module voltages converge simultaneously, and their maximum differences reduce to 48 mV and 51 mV, respectively. Equalizer turns off at point A, a weak battery recovery effect occurs due to the small balancing current according to the terminal voltages (in Fig. 17 (a)). Compared with the constant-current balancing technique , this recovery effect induced error has been mitigated effectively. Specifically, the voltage of cell with highest/lowest initial voltage value converges rapidly at the beginning of balancing process, and then the slope of voltage curves drops. This means higher voltage difference automatically exhibits a larger balancing current. This agrees with the analysis of current-converge characteristics in Section II. Since the balancing current is small near the balanced region (small voltage difference), it may take several hours to eliminate voltage difference of tens of millivolts. Thus, this equalizer stops when the voltage mismatch has been mitigated clearly, ensuring a comprise between the equalization speed and accuracy.

Balancing experiments during battery charging/discharging are also conducted. Figs. 18 and 19 show the voltage curves of the battery strings in constant-current charging and discharging

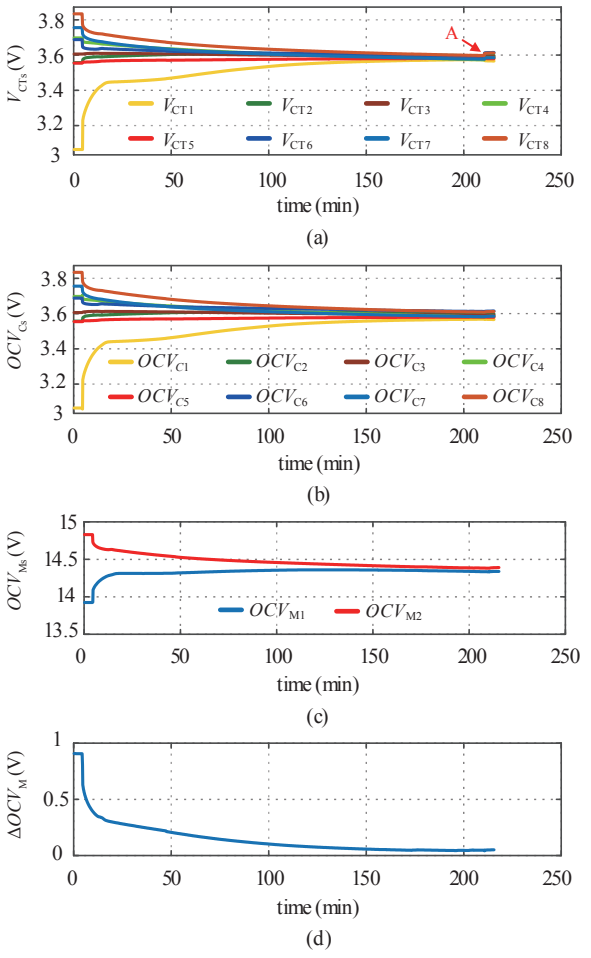


Fig. 17. Voltages with the cell string in static condition. (a) V_{CTs}, (b) OCV_{Cs}, (c) OCV_{Ms} and (d) ΔOCV_M.

conditions, respectively. In Fig. 18 (a), the voltages automatically and simultaneously converge to each other during the charging process, even with a changed charging current (before A: 100 mA, A-B: 150 mA). The charging process stops at point B, all cell exhibits a clear recovery effect while the voltage consistency is maintained well. This increases the rechargeable charge of battery string significantly. Similarly, at the condition of discharging with 150 mA, both cell and module voltages converge during the dropping process shown in Fig. 19 (a) and (b). This extends the discharge time of cell string and mitigates the voltage mismatch effectively. It should be noted that all the balancing processes are realized by a simple PWM driving signal with fixed f_s and D without the usage of SOC-estimation based control algorithm. This verifies the analysis and design of the proposed equalizer with open-loop control.

C. Performance Comparison

Table II illustrates a comparison of some typical equalizing methods, in terms of efficiency, switching frequency, balancing speed, accuracy, extendibility, control complexity and synchronization. The quantitative data sets such as efficiency, switch-

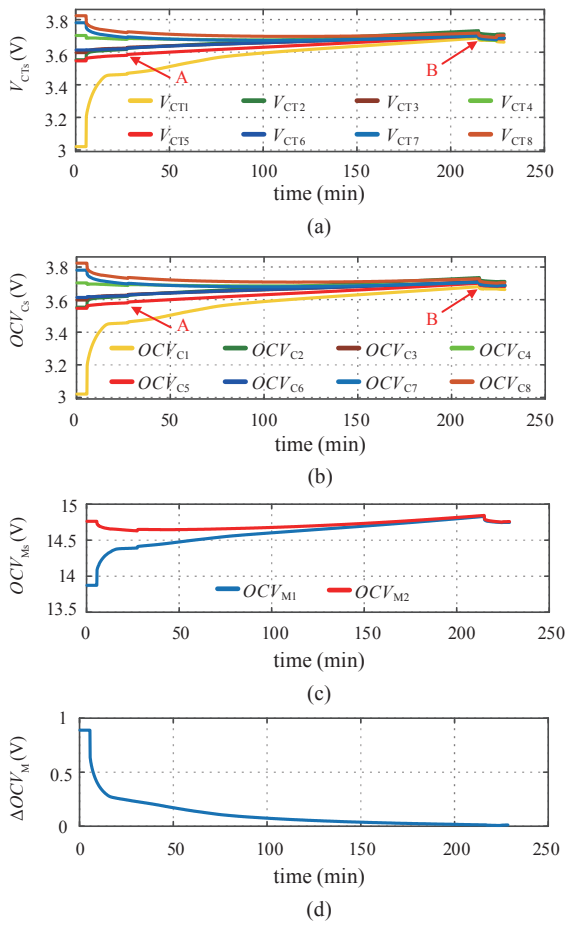


Fig. 18. Voltages with the cell string in charge condition. (a) V_{CTs}, (b) OCV_{Cs}, (c) OCV_{Ms} and (d) ΔOCV_{M}.

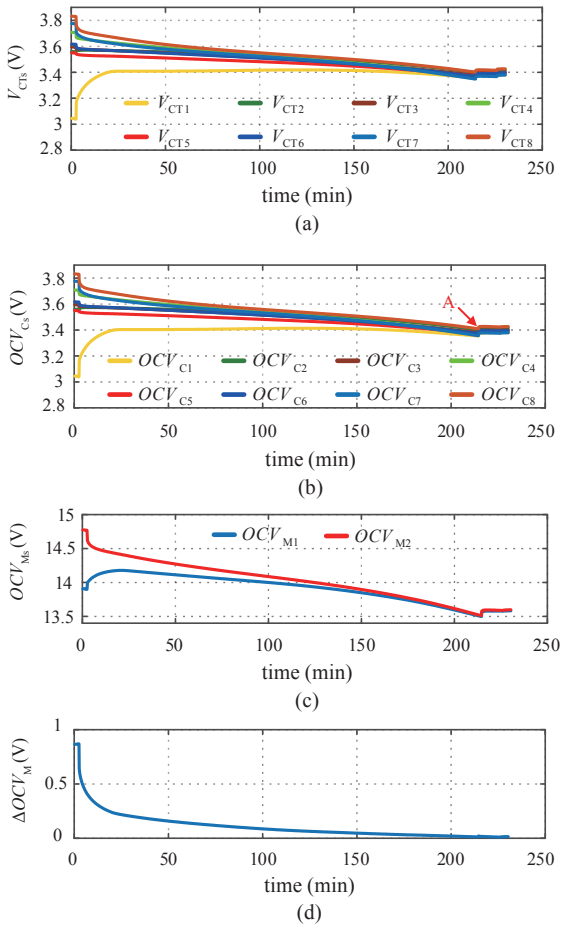


Fig. 19. Voltages with the cell string in discharge condition. (a) V_{CTs}, (b) OCV_{Cs}, (c) OCV_{Ms} and (d) ΔOCV_{M}.

ing frequency, balancing current and accuracy are extracted from experimental results. The remaining qualitative indicators use binary criteria (Yes or No). Efficiency is measured by the conversion efficiency of equalization circuit. For methods using hierarchical structures, like [4] and this work, the efficiency of each layer is listed. Switching frequency is also a critical parameter which affects the power density. For equalizers with similar efficiency, the design with higher switching frequency faciliates a more compact size. Balancing speed is evaluated by balancing current. Since the constant-current methods and the current-converge methods have essential difference, RMS current is used to reflect the balancing speed of the former case, while the peak current is used to reflect that of the latter ones. It is considered that with constant balancing current, the equalizer has faster balancing speed. Accuracy is evaluated by the voltage differences between cells near the balanced region, which reflects the ability of equalizer to resist the recovery effect. Extendibility is determined by circuit modularization and the feasibility in long battery string. The main consideration is the increase of equalizer units (or components) with the addition of cells. It is also noticed that some methods, such as multi-winding transformers, have structural limitations to extend, and this is also taken into account. Control complexity mainly considers whether SOC estimation is required. Synchronization is determined by whether cells can be balanced simultaneously.

As shown, in [1], the shunt resistor based passive equalizer exhibits excellent modularization and low control complexity. However, it suffers from zero efficiency and a relatively small balancing current. In [3], the hierarchical buck-boost converter based technique performs well in balancing speed. However, it needs SOC estimation to work in closed-loop to deal with the rocovery effect and to achieve a satisfactory accuracy. In [5], the multiphase interleaved converter demonstrates high efficiency and fast balancing speed, but poor equalization accuracy. In [6], the adjacent buck-boost equalizer achieves satisfactory accuracy at the cost of long energy-flow-paths. Meanwhile, it cannot equalize simultaneously. In [9], the switched-capacitor method exhibits high accuracy, excellent extendibility, and low control complexity. However, the switching frequency is low. In [14], the half-bidge based technique is introduced, but the efficiency and balancing speed is not satisfactory. Moreover, it suffers from poor extendibility because of the restriction of multi-winding transformer. In [22], with the utilization of VM, a high accuracy is achieved. Meanwhile, the efficiency is relatively high due to the external voltage source. In [18], a modular structure with a flyback converter is proposed,

TABLE II
COMPARISON OF DIFFERENT EQUALIZERS

References	[1]	[3]	[5]	[6]	[9]	[14]	[22]	[18]	[4]	This work
Equalization method	Passive method	C2C				S2C			Modular structure	
	Shunt resistor	Hierarchical buck-boost	Multiphase interleaved converter	Adjacent buck-boost	Switched-coupling-capacitor	Half-bridge	Voltage multiplier	Flyback	LLC & buck-boost	Half-bridge & buck-boost
Switching frequency/kHz	Unavailable	100	100	100	28.57	10	160	25	100	200
Efficiency/%	0	89.36	94	95	92.70	88	95	84.70	95.59 & 93.80	92.83 & 93.83
Balancing current/A	Unavailable	1 (RMS)	5 (Peak)	5 (Peak)	Unavailable	1.3 (Peak)	1.2 (Peak)	Unavailable	1 (RMS)	3 (Peak)
Accuracy/mV	Unavailable	25	100	20	10	Unavailable	6.2	12	14	48
Extendibility	Y	N	Y	Y	Y	N	Y	N	Y	Y
Control complexity (SOC estimation)	N	Y	N	N	N	N	N	N	Y	N
Synchronization	Y	N	Y	N	Y	Y	Y	Y	N	Y

which achieves a high accuracy. However, the efficiency is relatively low and the extendibility is poor because of the multi-winding transformer. In [4], a modular stucture combines LLC converter and buck-boost converter is investigated. The stucture outperforms in efficiency, balancing speed, accuracy, and extendibility. However, it needs SOC estimation to control the switches, which leads to high complexity and non-synchronization. In the proposed hybrid structure, the basic buck-boost converter ensures excellent extendibility. Meanwhile, combining with the half-bridge converter, a high efficiency and balancing speed can be achieved at a relatively high switching frequency. With the open-loop control method, the cells will be balanced simultaneously without SOC estimation, and the recovery effect is migitated.

IV. CONCLUSION

In this manuscript, a hierarchical modular battery equalizer with open-loop control and current-converge balancing is proposed. The module equalizer is based on half-bridge inverter and VM rectifier. It is combined with buck-boost based cell equalizer following the modular design concept. The operation principles and balancing features focusing on the balancing current of cell and module equalizer are analyzed in detail. The severe balancing error caused by battery recovery effect can be effectively and automatically mitigated using this current-converge balancing technique. The control only requires a pair of symmetrical PWM driving signals with fixed f_s and D without the SOC estimation and the detection of cell characteristics. This significantly reduces the control complexity and is easier to be extended to the large-scale energy storage systems with long battery string.

To evaluate the proposed concept, an experimental setup with eight series-connected batteries is built and tested. Both cell and module voltages can be automatically and simultaneously balanced when the battery string is in different working conditions of static, charging, and discharging. The voltage curves converge with a clearly mitigated recovery effect. The experimental results well validate the theoretical analysis of the proposed equalizer.

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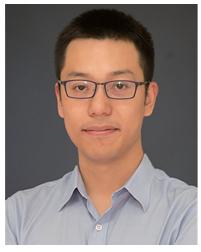

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