An H5-Bridge-Based Asymmetric *LLC* Resonant Converter With an Ultrawide Output Voltage Range

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***Abstract*—To extend the output voltage range of the conventional *LLC* topology, a small magnetizing inductance and a large frequency modulation window are required. Both would jeopardize the system performances. To resolve this issue, this article proposes a novel H5-bridge-based asymmetric *LLC* resonant converter. By configuring the switch pattern of the H5-bridge, two asymmetric *LLC* resonant tanks could operate in idle, half-bridge, hybrid-bridge, and full-bridge modes. Correspondingly, six operation modes with scaled voltage gains are obtained. Hence, an ultrawide output voltage range is achieved with moderate magnetizing inductance and simplified design of resonant parameters. The switching frequency range is squeezed close to the resonant frequency, which is beneficial for control implementation and circulating current suppression. Furthermore, two resonant tanks facilitate an easier zero-voltage switching (ZVS) of the primary-side MOSFETs and alleviate the current and voltage stresses. The conduction loss is further reduced due to the power-sharing effect between resonant tanks. To achieve a minimized frequency window, the optimized design of two resonant tanks is analyzed. To verify this concept, a 1-kW-rated prototype with 390 V input and 80–450 V output is designed and tested. Primary-side MOSFETs' ZVS are achieved over the entire load range. The designed prototype achieves 97.05% peak efficiency and good efficiency performance over the ultrawide output voltage range.**

***Index Terms*—Circuit reconfiguration, H5-bridge, *LLC*, wide output voltage range.**

I. Introduction

THE frequency-modulated (FM) *LLC* resonant converter is considered as a premium isolated dc–dc solution due to its

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1) zero-voltage switching (ZVS) on the primary MOSFETs,
2) low electromagnetic interference,
3) simple structure with low components count.

Thus, it is considered a candidate for the isolated dc–dc stage in plug-in electric vehicle (PEV) charging and other wide output voltage range applications [1]–[3].

To obtain a wide output voltage range using the conventional *LLC* topology, a small magnetizing inductance (L_m) and a wide switching frequency (f_s) window are required. The small L_m leads to large circulating current and conduction loss. Also, increasing f_s beyond the resonant frequency (f_r) bucks the normalized output voltage below unity. However, this leads to the loss of zero current switching (ZCS) on the secondary-side diodes and increased magnetic loss. On the other hand, reducing f_s below f_r boosts the normalized output voltage above unity. Nevertheless, low f_s leads to bulky magnetics and increased circulating loss. In general, operation close to f_r is defined as the optimal operation range with the optimum overall performance. Therefore, the state-of-the-art research on wide output voltage range *LLC* converters mainly focuses on squeezing the f_s span with moderate L_m.

Modifying the equivalent resonant parameters in different modes is able to extend the output voltage range. In [4], an auxiliary transformer with a current source is paralleled with the main transformer to adjust the equivalent L_m. In [5], an auxiliary capacitor is inserted into the transformer. Thus, the equivalent L_m can be modulated by f_s. Similarly, in [6], an *LC* structure is coupled with the transformer, such that the equivalent L_m could be adjusted by f_s. In a different perspective, modifying the equivalent C_r also helps to extend the output voltage range by adjusting the quality factor, Q. In [7], a controllable parallel resonant capacitor is introduced to the *LLC* topology. By configuring the ON/OFF state of the auxiliary MOSFET, Q is adjusted to obtain two suitable voltage gain profiles. However, modifying the equivalent resonant parameters might lead to low efficiency at light load [4], [8], increased design complexity [5], and steep gain-frequency profile [6]. Furthermore, it is difficult to optimize efficiency over the entire output voltage range.

Modifications in the control strategy can also extend the output voltage range. Both phase-shift (PS) control and pulsewidth modulation (PWM) are able to regulate the output voltage with constant f_s. In [9], an asymmetric PWM mechanism is introduced to regulate the output voltage. Similarly, in [9]–[13],

auxiliary PWM control is introduced to optimize the FM control. In [12], the *LLC* resonant tank operates in f_r, and a wide output voltage range is achieved by the PWM of the secondary-side MOSFET. In [14], an FM+PS control method is proposed. One phase leg of the rectifier is replaced by a synchronous rectifier (SR). Output voltage could be modulated by the PS between the SR and primary-side square wave. In [15], the normalized output voltage below unity is achieved by PS control. This helps to avoid the ZCS loss of FM with f_s beyond f_r and improves the voltage regulation capacity. On the other hand, the variable dc-link voltage also facilitates a squeezed f_s range [16]–[18]. The output voltage of the front-end PFC converter linearly tracks the output voltage. Thus, the second-stage *LLC* converter can always operate at the maximum efficiency point [19]. However, modifying the control strategy might lead to dc bias in magnetizing current [9] and increased current stress [14]. Moreover, the variable dc-link voltage technique presented in [19] requires a customized front-end ac–dc converter.

Reconfiguring the primary-side switch network can adjust the root-mean-square (rms) value of the resonant tank input voltage and effective turns ratio. Therefore, the output voltage range of the resonant converter can be extended conveniently. The most intuitive way is to implement the transition of the switching network between half-bridge and full-bridge configurations. Thus, a two-level voltage gain profile (1:2) is derived, and the smooth mode transition method is studied in [20]. Similar switch network reconfigurations are reported in [21]–[23]. In [22], a two-level voltage gain profile (1:1.5) is derived using two identical resonant tanks. In [23], a five-switch bridge is reconfigured to enable a four-step output voltage profile. However, this technique requires two identical resonant tanks, and the voltage range division is coarse. In [24], the transition between full-bridge rectifier and voltage doubler could extend the output voltage range. In [25], the transformer effective turns ratio could be adjusted by configuring the bidirectional auxiliary switch on the primary side. This two-level voltage gain profile facilitates extended output voltage and squeezed f_s window. In [26], both L_m and the effective turns ratio could be adjusted by configuring the bidirectional auxiliary switch. Thus, a four-level voltage gain profile is obtained to extend the output voltage range. In [27] and [28], different primary-side switch patterns are proposed to enable multiple voltage levels with modulated duty ratios. Hence, a multilevel voltage gain profile is realized to extend the output voltage range. Nevertheless, this method requires large counts number and complex driving signal.

In this article, an H5-bridge-based asymmetrical *LLC* resonant converter is proposed for wide output voltage range applications. Due to the H5-bridge structure, a six-step voltage gain profile is obtained. This effectively extends the output voltage range with further constrained f_s range. The advantages of the proposed converter include

1) six-step fine voltage gain division and ultrawide output voltage range,
2) narrow f_s range close to f_r,
3) relatively large L_m and low circulating current,
4) reduced primary-side conduction loss,
5) easy realization of ZVS,

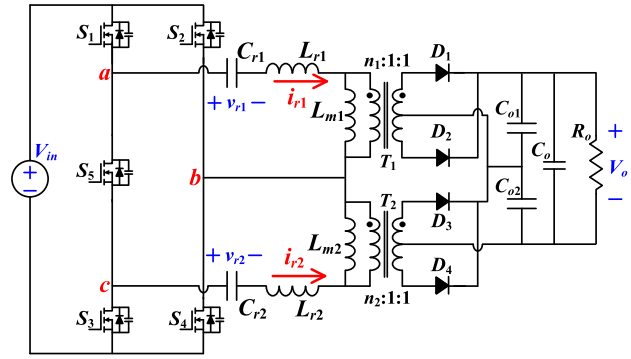

Fig. 1. Schematic of the proposed H5-bridge asymmetric *LLC* converter.

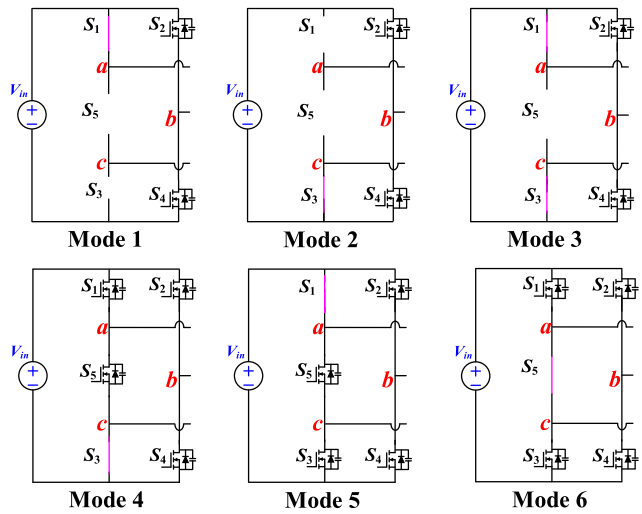

Fig. 2. Primary switch patterns in six modes.

6) alleviated current and voltage stresses in the resonant tanks,
7) elimination of the resonant current oscillations due to the split filtering capacitors.

II. Topological Description

Fig. 1 shows the schematic of the proposed converter. In comparison with the conventional full-bridge *LLC* resonant converter, an extra MOSFET is added on the primary side to enable a reconfigurable H5-bridge. The output of the H5-bridge is fed to two asymmetric *LLC* resonant tanks with a different set of resonant parameters. In those two resonant tanks, the resonant inductance (L_{r1} and L_{r2}), resonant capacitance (C_{r1} and C_{r2}), magnetizing inductance (L_{m1} and L_{m2}), and transformers' turns ratio (n_1 and n_2) are all different. The secondary side is two center-tapped transformer-based full-wave rectifiers. The outputs of those two rectifiers are in series. The rms values of the two *LLC* resonant tanks' input voltages ($v_{ab,\mathrm{rms}}$ and $v_{cb,\mathrm{rms}}$), could be easily adjusted by configuring the primary-side MOSFETs among ON state, OFF state, and FM state. Hence, a six-step voltage gain profile could be derived.

The switch patterns of the H5-bridge, which correspond to six voltage gain profiles, are plotted in Fig. 2. The corresponding

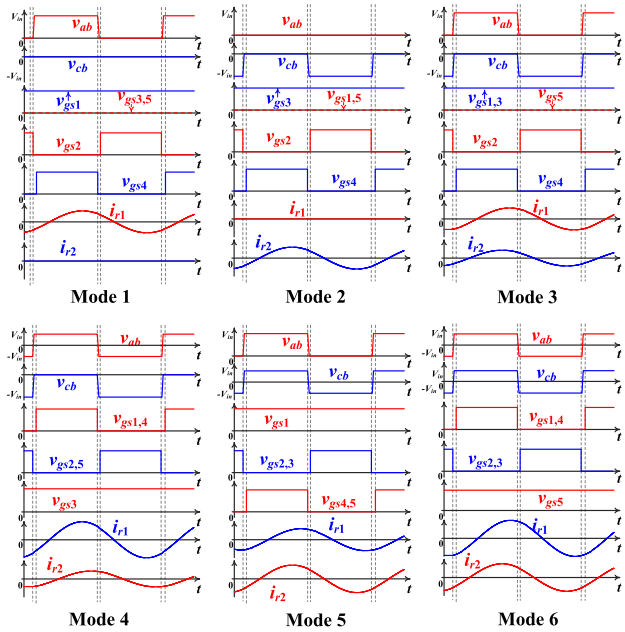

Fig. 3. Key steady-state waveforms in six modes.

key steady-state waveforms are plotted in Fig. 3. As shown in the figure, the proposed topology enables six different operation modes.

Mode 1: In this mode, S_1 is always ON, and $S_{3,5}$ are always OFF. S_2 and S_4 are driven complementarily with certain deadband (FM state). Resonant tank 2 (RT2) is disabled and does not transfer power to the output. Resonant tank 1 (RT1) is in half-bridge mode since its input voltage, v_{ab}, is a two-level square wave (0 V to V_{in}) and $v_{ab,\text{rms}}$ is $V_{\text{in}}/2$.

Mode 2: In this mode, S_3 is always ON, and $S_{1,5}$ are always off. S_2 and S_4 operate in the FM state. Similarly, RT1 is disabled and does not transfer power to the output. RT2 is in the half-bridge mode since its input voltage, v_{cb}, is a two-level square wave ($-V_{\text{in}}$ to 0 V) and $v_{cb,\text{rms}}$ is $V_{\text{in}}/2$. Since n_1 and n_2 are unequal, voltage gain profiles in modes 1 and 2 are different.

Mode 3: In this mode, $S_{1,3}$ are always ON, and S_5 is always OFF. S_2 and S_4 operate in the FM state. v_{ab} and v_{cb} are two-level square waves (0 V to V_{in}, $-V_{\text{in}}$ to 0 V). Both $v_{ab,\text{rms}}$ and $v_{cb,\text{rms}}$ are $V_{\text{in}}/2$. Hence, both RT1 and RT2 are in the half-bridge mode. Due to different turns ratio, the power transferred via two resonant tanks are also different. Since n_2 is smaller than n_1, RT2 transfers more power than RT1 does.

Mode 4: In this mode, S_3 is always ON. $S_{2,5}$ and $S_{1,4}$ operate in the FM state. v_{ab} and v_{cb} are two-level square waves ($-V_{\text{in}}$ to V_{in}, $-V_{\text{in}}$ to 0 V). $v_{ab,\text{rms}}$ is V_{in}, whereas $v_{cb,\text{rms}}$ is $V_{\text{in}}/2$. Hence, RT1 is in the full-bridge mode, and RT2 is in the half-bridge mode. In this mode, RT1 transfers more power since $v_{ab,\text{rms}}$ equals $2v_{cb,\text{rms}}$.

Mode 5: In this mode, S_1 is always ON. $S_{2,3}$ and $S_{4,5}$ operate in the FM state. v_{ab} and v_{cb} are two-level square waves (0 V to V_{in}, $-V_{\text{in}}$ to V_{in}). $v_{ab,\text{rms}}$ is $V_{\text{in}}/2$, whereas $v_{cb,\text{rms}}$ is V_{in}. Hence, RT1 is in the half-bridge mode, and RT2 is in the full-bridge mode. Due to the smaller n_2 and larger input voltage rms value, RT2 transfers more power than RT1. Similarly, since n_1 and n_2 are unequal, voltage gain profiles in modes 4 and 5 are different.

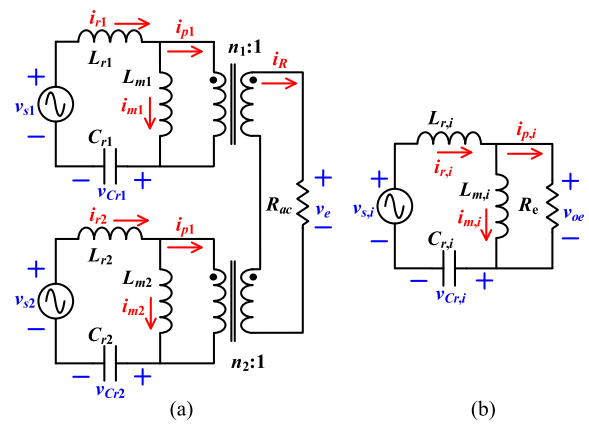

Fig. 4. (a) General equivalent circuit model in six modes. (b) Equivalent circuit model for modes 1 and 2.

Mode 6: In this mode, S_5 is always ON. $S_{2,3}$ and $S_{1,4}$ operate in the FM state. v_{ab} and v_{cb} are two-level square waves ($-V_{\text{in}}$ to V_{in}). $v_{ab,\text{rms}}$ and $v_{cb,\text{rms}}$ are both V_{in}. Hence, both RT1 and RT2 are in the full-bridge mode. The proposed converter achieves the largest output voltage in this mode. Since n_2 is smaller than n_1, RT2 transfers more power than RT1.

III. Modeling and Analysis

A. Circuit Modeling

Since f_s range is squeezed and close to f_r, the first-harmonic-analysis (FHA) method maintains good modeling accuracy. Thus, FHA is adopted to construct the equivalent circuit model in six modes. The general equivalent circuits model of the proposed converter is plotted in Fig. 4(a). As shown in the figure, v_{s1} and v_{s2} are the fundamental frequency components of v_{ab} and v_{cb}, respectively. R_{ac} and v_e are the equivalent load and output voltage. In modes 1 and 2, only one resonant tank is enabled. Therefore, the equivalent circuit model can be simplified, as shown in Fig. 4(b).

In modes 3–6, both RT1 and RT2 are enabled. To simplify the analysis, the output is split according to the power shares of two resonant tank. The resulting circuit model is plotted in Fig. 5(a). In Fig. 5(a), points d and e have equal voltage potential. Thus, the equivalent circuit models in modes 3–6 can be merged, as shown in Fig. 5(b). It can be regarded as two separate *LLC* resonant converters with $n_1 i_{p1} = n_2 i_{p2}$

$$R_{e1} = n_1^2 R_{ac1} \tag{1}$$

$$R_{e2} = n_2^2 R_{ac2} \tag{2}$$

$$R_{ac1} + R_{ac2} = R_{ac}. \tag{3}$$

The conventional *LLC* resonant converters have been well studied in literature. To simplify the analysis, this article mainly focuses on the uniqueness of the proposed converter.

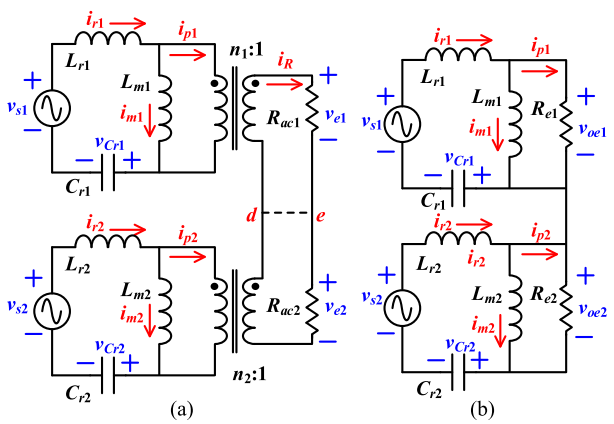

Fig. 5. Equivalent circuit model for modes 3–6 with (a) series load and (b) split load.

B. Voltage Gain Analysis

1) Modes 1 and 2: In mode 1, only RT1 is enabled. Hence, all output voltage is applied to RT1's secondary side, and the following state equation is obtained:

$$\begin{aligned}\frac{dv_{Cr1}}{dt} &= i_{Lr1}/C_{r1}\\ \frac{di_{Lr1}}{dt} &= (v_{s1} - v_{Cr1} - n_1 v_e)/L_{r1}\\ \frac{di_{m1}}{dt} &= n_1 v_e/L_{m1}.\end{aligned} \tag{4}$$

Similarly, the following state equation in mode 2 is derived:

$$\begin{aligned}\frac{dv_{Cr2}}{dt} &= i_{Lr2}/C_{r2}\\ \frac{di_{Lr2}}{dt} &= (v_{s2} - v_{Cr2} - n_2 v_e)/L_{r2}\\ \frac{di_{m2}}{dt} &= n_2 v_e/L_{m2}.\end{aligned} \tag{5}$$

According to (4) and (5), the state equations in modes 1 and 2 are identical to those in conventional *LLC* resonant converter. V_o is the total output voltage, or the load terminal voltage; V_{in} is the input voltage, or the source terminal voltage. Therefore, the voltage gains at f_r in those two modes are

$$G_1 = \frac{V_o}{V_{\text{in}}} = \frac{1}{2n_1}, \quad \text{Mode 1} \tag{6}$$

$$G_2 = \frac{V_o}{V_{\text{in}}} = \frac{1}{2n_2}, \quad \text{Mode 2.} \tag{7}$$

2) Modes 3–6: In modes 3–6, both *LLC* resonant tanks are enabled. According to the circuit model shown in Fig. 5(a), the state equations in modes 3–6 are derived as follows:

$$\begin{aligned}\frac{dv_{Cr1}}{dt} &= i_{Lr1}/C_{r1}\\ \frac{di_{Lr1}}{dt} &= (v_{s1} - v_{Cr1} - n_1 v_{e1})/L_{r1}\\ \frac{di_{m1}}{dt} &= n_1 v_{e1}/L_{m1}\end{aligned} \tag{8}$$

TABLE I
VOLTAGE GAINS AT RESONANT FREQUENCY IN SIX MODES

Modes	Tanks	$v_{ab,rms}$	$v_{cb,rms}$	*Gain*
Mode 1	1	$V_{in}/2$	0	G_0
Mode 2	1	0	$V_{in}/2$	$(n_1/n_2)G_0$
Mode 3	2	$V_{in}/2$	$V_{in}/2$	$(1+n_1/n_2)G_0$
Mode 4	2	V_{in}	$V_{in}/2$	$(2+n_1/n_2)G_0$
Mode 5	2	$V_{in}/2$	V_{in}	$(1+2n_1/n_2)G_0$
Mode 6	2	V_{in}	V_{in}	$(2+2n_1/n_2)G_0$

$$\begin{aligned}\frac{dv_{Cr2}}{dt} &= i_{Lr2}/C_{r2}\\ \frac{di_{Lr2}}{dt} &= (v_{s2} - v_{Cr2} - n_2 v_{e2})/L_{r2}\\ \frac{di_{m2}}{dt} &= n_2 v_{e2}/L_{m2}.\end{aligned} \tag{9}$$

According to (8) and (9), the state equations of two *LLC* resonant tanks are also identical to the conventional *LLC* resonant converter. Therefore, the voltage gains in modes 3–6 equals the sum of the voltage gains of two separate *LLC* resonant converters. It should be noted that the *LLC* resonant tank operates at full-bridge mode or half-bridge mode. The voltage gains at f_r in modes 3–6 are expressed as follows:

$$G_3 = \frac{1}{2n_1} + \frac{1}{2n_2}, \quad \text{Mode 3} \tag{10}$$

$$G_4 = \frac{1}{n_1} + \frac{1}{2n_2}, \quad \text{Mode 4} \tag{11}$$

$$G_5 = \frac{1}{2n_1} + \frac{1}{n_2}, \quad \text{Mode 5} \tag{12}$$

$$G_6 = \frac{1}{n_1} + \frac{1}{n_2}, \quad \text{Mode 6.} \tag{13}$$

The voltage gains in six modes are summarized in Table I. In the range where f_s is unequal to f_r, the voltage gains are

$$G = G_{f_s=f_r} f(Q, m, f_n) \tag{14}$$

$$f(Q, m, f_n) = \frac{m f_n^2}{\sqrt{\left[(m+1)f_n^2 - 1\right]^2 + m^2 Q^2 f_n^2 (f_n^2 - 1)^2}} \tag{15}$$

$$Q = \frac{\sqrt{L_r/C_r}}{R_L 8n^2/\pi^2} \tag{16}$$

where f_n is the normalized frequency, and m is the inductance ratio. All are identical to those in conventional *LLC* resonant converters. In modes 1 and 2, R_L equals R_o. In modes 3–6, R_L is part of the R_o. The corresponding voltage gain curves in six modes and the operation range are plotted in Fig. 6. As shown in the figure, the six-step voltage gain profile is generated by six modes. It enables both a much-extended output voltage range and an effectively squeezed f_s window. Due to the facts a) f_s is close to f_r, and b) Q and m are properly designed following the flowchart illustrated in Fig. 7, the voltage gains of the proposed converter in six modes are scaled, as indicated in Table I.

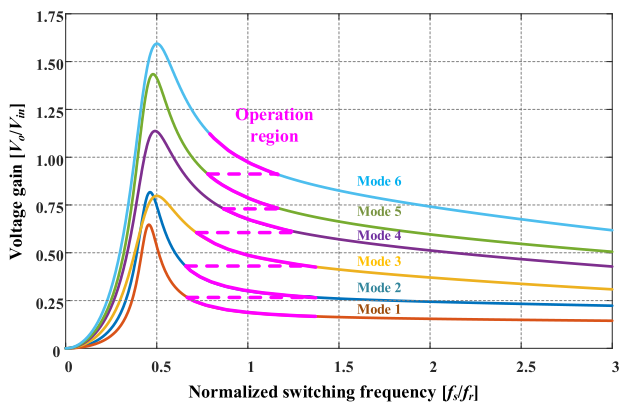

Fig. 6. Voltage gain curves in six modes.

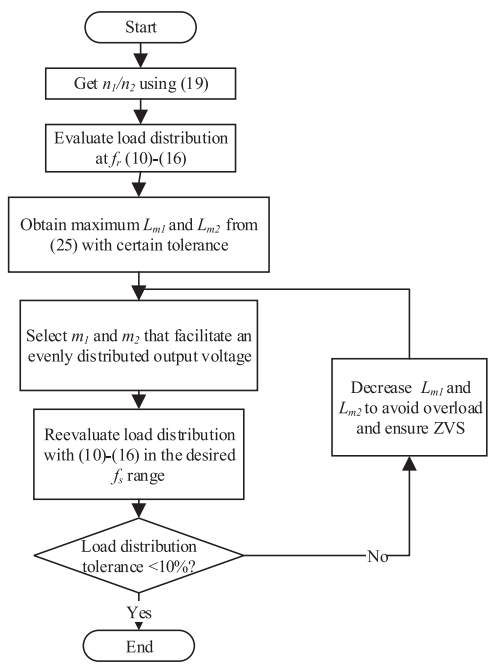

Fig. 7. Flowchart to design quality factor (Q) and inductance ratio (m).

Since wide output voltage range is achieved by the six-step voltage gain profile with moderate L_m and narrow f_s span, the large conduction loss, circulating loss, and bulky magnetic component caused by small L_m and wide f_s span are avoided. The conduction loss introduced by the extra MOSFET is smaller than the reduced conduction and circulating loss.

IV. Critical Design Considerations

A. Narrowest f_s Range and Turns Ratio

To obtain a narrowest overall f_s range, the f_s range in six modes should be distributed uniformly. Assuming the peak and valley voltage gains in mode 1 are x and y, respectively. According to the voltage gain analysis presented in Section III-B, the peak and valley voltage gains in modes 2–6 can be obtained, as shown in Table II.

TABLE II
Voltage Gain Range in Each Mode

Modes	Peak gain	Valley gain
Mode 1	x	y
Mode 2	$(n_1/n_2)x$	$(n_1/n_2)y$
Mode 3	$(1+n_1/n_2)x$	$(1+n_1/n_2)y$
Mode 4	$(2+n_1/n_2)x$	$(2+n_1/n_2)y$
Mode 5	$(1+2n_1/n_2)x$	$(1+2n_1/n_2)y$
Mode 6	$(2+2n_1/n_2)x$	$(2+2n_1/n_2)y$

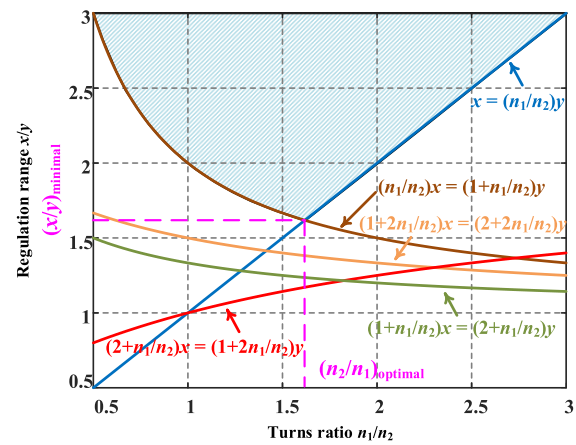

Fig. 8. n_1/n_2's impact on required voltage regulation range.

To provide a continuous voltage gain profile, the peak voltage gain in the previous mode should be larger than the valley voltage gain in the next mode

$$\begin{aligned} x &\geq (n_1/n_2)\,y \\ (n_1/n_2)\,x &\geq (1+n_1/n_2)\,y \\ (1+n_1/n_2)\,x &\geq (2+n_1/n_2)\,y \\ (2+n_1/n_2)\,x &\geq (1+2n_1/n_2)\,y \\ (1+2n_1/n_2)\,x &\geq (2+2n_1/n_2)\,y. \end{aligned} \tag{17}$$

To make the f_s range narrowest, the voltage regulation range should be optimized

$$\begin{aligned} x/y \geq [&n_1/n_2, 1+n_2/n_1, (n_1+2n_2)/(n_1+n_2), \\ &(2n_1+n_2)/(n_1+2n_2), (2n_1+2n_2)/(2n_1+n_2)]_{\max}. \end{aligned} \tag{18}$$

The impact of n_1/n_2 on required voltage regulation range is shown in Fig. 8. From (18) and Fig. 8, the smallest x/y and narrowest f_s range could be achieved with optimal n_2/n_1

$$(n_1/n_2)_{\text{optimal}} = \frac{1+\sqrt{5}}{2} \approx 1.62. \tag{19}$$

B. ZVS Condition

The i_r, i_m, and v_{in} in the conventional *LLC* resonant converter at f_r are plotted in Fig. 9. I_m is the peak value of i_m

$$i_r(T_s/2) = i_m(T_s/2) = I_m \tag{20}$$

$$I_m = \frac{nV_o}{4L_m f_s}. \tag{21}$$

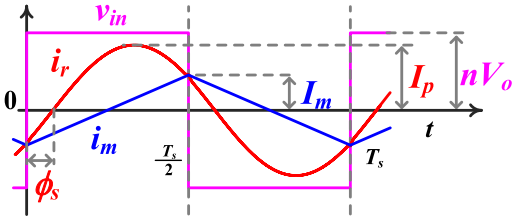

Fig. 9. i_r and i_m in the conventional full-bridge *LLC* converter.

To realize the ZVS of the primary MOSFETs, i_r should be sufficiently large to fully charge and discharge the MOSFETs' output capacitor during the deadband [29]. t_d is the duration of deadband. C_{oss} is the energy-normalized output capacitance

$$I_m t_d > 2C_{\text{oss}} V_{\text{in}} \tag{22}$$

$$t_d \geq \frac{8L_m C_{\text{oss}} f_s V_{\text{in}}}{nV_o}. \tag{23}$$

1) Modes 1 and 2: As shown in Fig. 4(b), the equivalent circuit model in modes 1 and 2 is identical to that of the conventional *LLC* resonant converter. Hence, their ZVS conditions are the same

$$\begin{cases} t_d \geq \dfrac{8L_{m1} C_{\text{oss}} f_s V_{\text{in}}}{n_1 V_o}, & \text{Mode 1} \\ t_d \geq \dfrac{8L_{m2} C_{\text{oss}} f_s V_{\text{in}}}{n_2 V_o}, & \text{Mode 2} \end{cases}. \tag{24}$$

Both *LLC* resonant tanks operate in the half-bridge mode, $nV_o = V_{\text{in}}/2$

$$\begin{cases} t_d \geq 16L_{m1} C_{\text{oss}} f_s, & \text{Mode 1} \\ t_d \geq 16L_{m2} C_{\text{oss}} f_s, & \text{Mode 2} \end{cases}. \tag{25}$$

2) Modes 3–6: In modes 3–6, i_r of both *LLC* resonant tanks charge and discharge the MOSFETs' C_{oss}

$$(I_{m1} + I_{m2})\, t_d > 2C_{\text{oss}} V_{\text{in}}. \tag{26}$$

According to the equivalent circuit model in modes (3)–(6) and (21)

$$\left(\frac{n_1 V_1}{4L_{m1} f_s} + \frac{n_2 V_2}{4L_{m2} f_s}\right) t_d > 2C_{\text{oss}} V_{\text{in}} \tag{27}$$

$$n_1 V_1 = n_2 V_2 = V_{\text{in}}/2, \quad \text{Mode 3} \tag{28}$$

$$n_1 V_1 = 2n_2 V_2 = V_{\text{in}}, \quad \text{Mode 4} \tag{29}$$

$$n_2 V_2 = 2n_1 V_1 = V_{\text{in}}, \quad \text{Mode 5} \tag{30}$$

$$n_1 V_1 = n_2 V_2 = V_{\text{in}}, \quad \text{Mode 6}. \tag{31}$$

Therefore, the ZVS conditions for primary-side MOSFETs in modes 3–6 can be obtained and are given as follows:

$$t_d > 16C_{\text{oss}} f_s \frac{L_{m1} L_{m2}}{L_{m1} + L_{m2}}, \quad \text{Mode 3} \tag{32}$$

$$t_d > 16C_{\text{oss}} f_s \frac{L_{m1} L_{m2}}{L_{m1} + 2L_{m2}}, \quad \text{Mode 4} \tag{33}$$

$$t_d > 16C_{\text{oss}} f_s \frac{L_{m1} L_{m2}}{2L_{m1} + L_{m2}}, \quad \text{Mode 5} \tag{34}$$

$$t_d > 8C_{\text{oss}} f_s \frac{L_{m1} L_{m2}}{L_{m1} + L_{m2}}, \quad \text{Mode 6}. \tag{35}$$

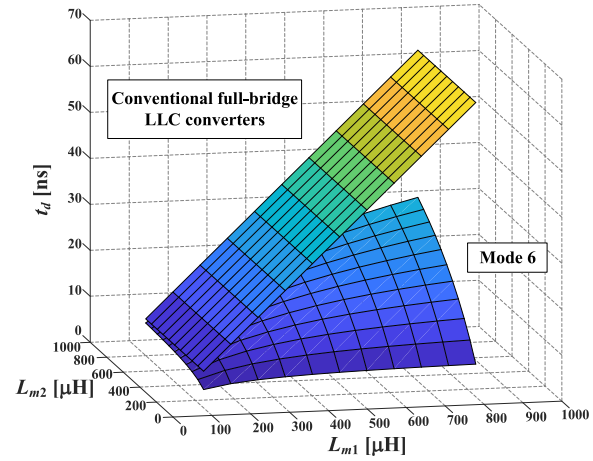

Fig. 10. t_d to achieve the ZVS of primary-side MOSFETs.

TABLE III
POWER DISTRIBUTION BETWEEN TWO RESONANT TANKS

Modes	P_{o1}/P_o	P_{o2}/P_o
Mode 1	100%	0
Mode 2	0	100%
Mode 3	$n_2/(n_1+n_2)$	$n_1/(n_1+n_2)$
Mode 4	$2n_2/(n_1+2n_2)$	$n_1/(n_1+2n_2)$
Mode 5	$n_2/(2n_1+n_2)$	$2n_1/(2n_1+n_2)$
Mode 6	$n_2/(n_1+n_2)$	$n_1/(n_1+n_2)$

The required t_d to realize ZVS for conventional full-bridge *LLC* converters and the proposed converter in mode 6 are compared graphically in Fig. 10. The L_{m1} and L_{m2} in Fig. 10 of the conventional *LLC* converter are same and equal to the L_m of the conventional *LLC* converter. It can be found that the t_d is reduced in our proposed converter. This is because both resonant tanks contribute currents to charge and discharge the C_{oss}. This is also beneficial to reduce L_m.

The conduction loss of primary side is expressed as follows:

$$P_{\text{con}} = i_r^2 r_p \tag{36}$$

where r_p is the equivalent primary-side resistance, including wire resistance and copper resistance of magnetic components. The conduction loss is reduced because i_r is split between two *LLC* resonant tanks.

In mode 1, only resonant tank 1 is enabled, whereas in mode 2, only resonant tanks 2 is enabled. Hence, in modes 1 and 2, the enabled resonant tank carries all the power.

In modes 3–6, both resonant tanks are enabled. Nevertheless, due to the asymmetric resonant parameters, the power shares of two resonant tanks are unmatched. On the secondary side, two resonant tanks' currents are identical. Hence, the power distribution between two resonant tanks equals their voltage distribution. Based on the voltage gain analysis presented in Section III-B, the output voltage difference between two resonant tanks origins from different turns ratios and different $v_{\text{in,rms}}$. Correspondingly, the power distribution between two resonant tanks is summarized in Table III.

According to Table III, the power delivered via each resonant tank varies with output power and operating modes. The maximum power carried by each resonant tank should be decided by specific n_1/n_2 and power range in each mode.

C. Electric Stresses

According to Fig. 8, the peak current of i_r and I_p in the *LLC* resonant converter is derived as follows:

$$I_p = \sqrt{\frac{\pi^2 V_o^2}{4n^2 R_o^2} + \frac{n^2 V_o^2}{16 L_m^2 f_s^2}}. \tag{37}$$

1) Modes 1 and 2: According to (37) and the equivalent circuits shown in Fig. 5(b), I_p in modes 1 and 2 is derived as follows:

$$I_p = \sqrt{\frac{\pi^2 V_o^2}{4n_1^2 R_o^2} + \frac{n_1^2 V_o^2}{16 L_{m1}^2 f_s^2}} \quad \text{Mode 1} \tag{38}$$

$$I_p = \sqrt{\frac{\pi^2 V_o^2}{4n_2^2 R_o^2} + \frac{n_2^2 V_o^2}{16 L_{m2}^2 f_s^2}} \quad \text{Mode 2.} \tag{39}$$

2) Modes 3–6: The current delivered to the secondary-side equals $i_r - i_m$. Also, at $t = 0$, $i_r = i_m$. I_{p1} and I_{p2} are the peak values of i_{r1} and i_{r2}, respectively

$$\frac{2}{T_s}\int_0^{\frac{T_s}{2}} \left(I_{p1}\sin(\omega_s t - \varphi_{s1}) - \frac{n_1 V_1}{L_{m1} f_s} t + \frac{n_1 V_1}{4 L_{m1} f_s}\right) dt = \frac{V_o}{n_1 R_o} \tag{40}$$

$$\frac{2}{T_s}\int_0^{\frac{T_s}{2}} \left(I_{p2}\sin(\omega_s t - \varphi_{s2}) - \frac{n_2 V_2}{L_{m2} f_s} t + \frac{n_2 V_2}{4 L_{m2} f_s}\right) dt = \frac{V_o}{n_2 R_o} \tag{41}$$

$$I_{p1}\sin(-\varphi_{s1}) = -\frac{n_1 V_1}{4 L_{m1} f_s} \tag{42}$$

$$I_{p2}\sin(-\varphi_{s2}) = -\frac{n_2 V_2}{4 L_{m2} f_s}. \tag{43}$$

Based on the power distribution obtained in Section IV-C, V_1/V_o and V_2/V_o are derived. Correspondingly, I_p in each resonant tank in modes 3–6 is derived as follows:

$$\begin{cases} I_{p1} = \sqrt{\frac{\pi^2 V_o^2}{4n_1^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{16 L_{m1}^2 f_s^2 (n_1+n_2)^2}} \\ I_{p2} = \sqrt{\frac{\pi^2 V_o^2}{4n_2^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{16 L_{m2}^2 f_s^2 (n_1+n_2)^2}} \end{cases} \quad \text{Mode 3} \tag{44}$$

$$\begin{cases} I_{p1} = \sqrt{\frac{\pi^2 V_o^2}{4n_1^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{4 L_{m1}^2 f_s^2 (n_1+2n_2)^2}} \\ I_{p2} = \sqrt{\frac{\pi^2 V_o^2}{4n_2^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{16 L_{m2}^2 f_s^2 (n_1+2n_2)^2}} \end{cases} \quad \text{Mode 4} \tag{45}$$

$$\begin{cases} I_{p1} = \sqrt{\frac{\pi^2 V_o^2}{4n_1^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{16 L_{m1}^2 f_s^2 (2n_1+n_2)^2}} \\ I_{p2} = \sqrt{\frac{\pi^2 V_o^2}{4n_2^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{4 L_{m2}^2 f_s^2 (2n_1+n_2)^2}} \end{cases} \quad \text{Mode 5} \tag{46}$$

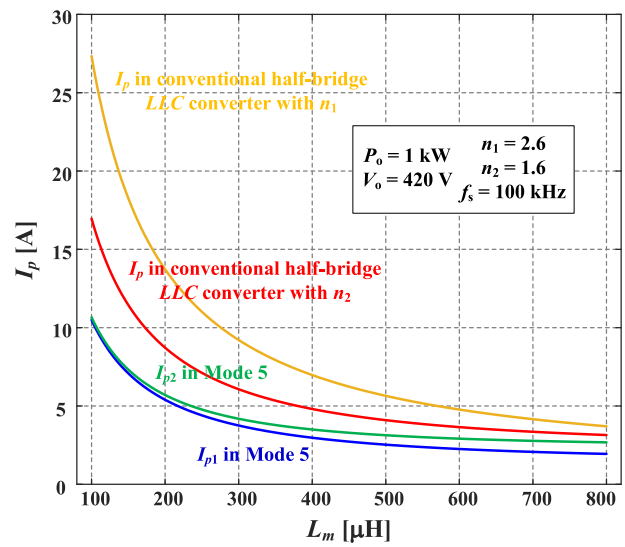

Fig. 11. Comparison of primary-side peak currents.

$$\begin{cases} I_{p1} = \sqrt{\frac{\pi^2 V_o^2}{4n_1^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{16 L_{m1}^2 f_s^2 (n_1+n_2)^2}} \\ I_{p2} = \sqrt{\frac{\pi^2 V_o^2}{4n_2^2 R_o^2} + \frac{n_1^2 n_2^2 V_o^2}{16 L_{m2}^2 f_s^2 (n_1+n_2)^2}} \end{cases} \quad \text{Mode 6.} \tag{47}$$

I_{p1} and I_{p2} are the peak currents in two resonant tanks, respectively. It can be found that the expressions of peak current in modes 3 and 6 are identical. This is because V_1/V_o and V_2/V_o in these two modes are identical.

According to the comparison of primary-side peak currents, as shown in Fig. 11, the current stress of the proposed converter is reduced. This reduction is more obvious with larger L_m, which is the benefit of the proposed converter. Due to the resonance between L_r and C_r, a similar result for voltage stress in C_r could be derived

$$V_{rp} = \sqrt{I_p^2 L_r / C_r} \tag{48}$$

V_{rp} is the peak voltage in C_r.

D. Attractive Features

1) Low Circulating Current Loss: For *LLC* converters, certain circulating current is required to facilitate the ZVS turning ON of the primary-side MOSFETs. During each mode, the sum of currents of L_{m1} and L_{m2} contributes to the charging current to realized ZVS in the deadband, as shown in (26). Accordingly, to make a fair comparison between the proposed converter and conventional *LLC* converter, the following assumption is made:

$$I_{m1} + I_{m2} = I_{m,\text{conv}} \tag{49}$$

where $I_{m,\text{conv}}$ is the circulating current of the conventional *LLC* converter. It is obvious that $I_{m1}^2 + I_{m2}^2$ is smaller than $(I_{m1} + I_{m2})^2$. Since the circulating loss is proportional to the square of charging currents, we can judge that the circulating loss of the proposed converter is reduced.

For instance, assume each resonant tank resistance is approximately equal to R_{tank}. If we use a 3 A current to charge the output

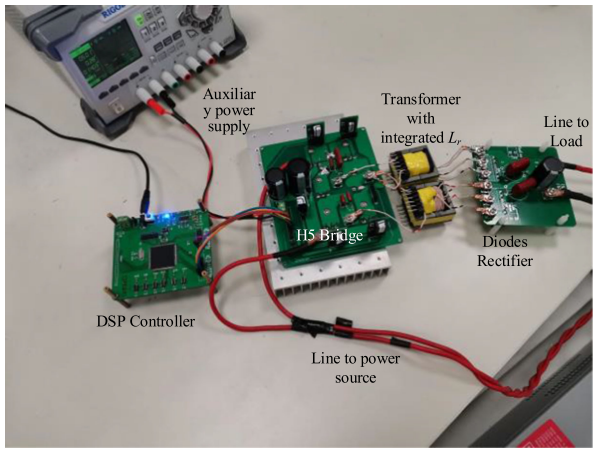

Fig. 12. Photograph of the designed prototype.

capacitor of MOSFETs in the deadband for ZVS, the conduction loss in the resonant tank for conventional *LLC* is $9R_{\text{tank}}$; but in H5 topology, if RT1 has half of charging current, like 1.5 A, and RT2 has another half charging current, total loss of H5 bridge is $4.5R_{\text{tank}}$. Conduction loss is reduced about 50%.

2) Easy Realization of ZVS: In a different perspective, with the same circulating power loss, the following assumption should hold:

$$I_{m1}{}^2 + I_{m2}{}^2 = I_{m,\text{conv}}{}^2. \tag{50}$$

Accordingly, the following relationship is derived:

$$(I_{m1} + I_{m2}) > \sqrt{I_{m1}{}^2 + I_{m2}{}^2} = \sqrt{I_{m,\text{conv}}{}^2} = I_{m,\text{conv}}. \tag{51}$$

Since $I_{m1} + I_{m2} > I_{m,\text{conv}}$, we can judge that the proposed converter enables an easier realization of ZVS.

Similarly, if we limit the circulating loss, like $9R_{\text{tank}}$, for the conventional half-bridge *LLC* converter, it provides a device whose $Q_o = 3t_d/2$, where t_d is the deadtime to achieve ZVS. For H5 *LLC*, if RT1 current equals RT2 current, then the total charge will be $4.24t_d/2$. The charge is increased about 40%. Thus, the ZVS realization is easier.

3) Elimination of the Resonant Current Oscillations: The diode junction capacitance might affect the transformer secondary current. During the commutation process between diodes, the output voltages of both RT1 and RT2 are unclamped. Therefore, an oscillation might occur in i_{Lm}, which leads to the oscillation in i_{Lr}. In this article, two series-connected capacitors are installed to clamp the output voltage of RT1 and RT2. Thus, the oscillation is effectively eliminated.

V. Experimental Verification

To verify the effectiveness of the proposed converter, a 1-kW, 390 V input, 80–450 V output prototype converter for PEV charging applications is designed, as shown in Fig. 12. The specifications and design parameters of the prototype are listed in Table IV.

TABLE IV
Design Parameters of the Prototype

Symbol	Quantity	Parameters
V_{in}	Input voltage	390 V
V_o	Output voltage	80 - 450 V
L_{m1}, L_{m2}	Magnetizing inductance	287 μH, 264 μH
L_{r1}, L_{r2}	Resonant inductance	78 μH, 58 μH
C_{r1}, C_{r2}	Resonant capacitance	32 nF, 44 nF
n_1, n_2	Turns ratio	2.6, 1.6
$Q_{1\text{-}6}$	MOSFET switch	SCT3120AL
$D_{1\text{-}4}$	Rectifier diode	C3D10060A
f_r	Resonant frequency	100 kHz
f_s	Switching frequency	70 - 130 kHz
C_o, C_{o1}, C_{o2}	Output filter capacitor	1 μF, 1 μF, 100 μF

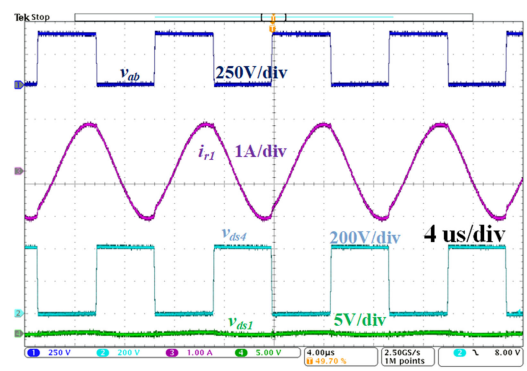

Fig. 13. Steady-state waveforms in mode 1 with $V_o = 84$ V and $P_o = 40$ W.

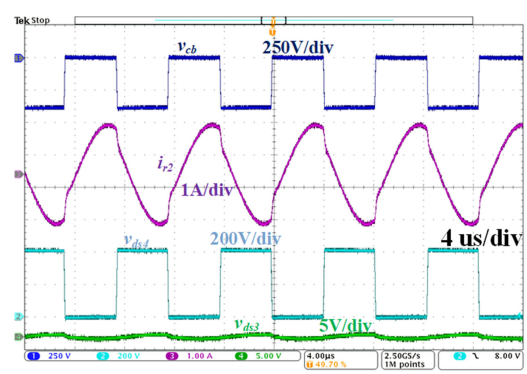

Fig. 14. Steady-state waveforms in mode 2 with $V_o = 120$ V and $P_o = 80$ W.

The steady-state waveforms in mode 1 are shown in Fig. 13. In this mode, v_{ab} is a two-level square wave (0–390 V). RT1 operates in the half-bridge mode. S_1 is always ON. There is no power transferred via RT2.

The steady-state waveforms in mode 2 are shown in Fig. 14. In this mode, v_{cb} is a two-level square wave (-390 to 0 V). RT2 operates in the half-bridge mode. S_3 is always ON. There is no power transferred via RT1.

The steady-state waveforms in mode 3 are shown in Fig. 15. In this mode, v_{ab} and v_{cb} are both two-level square waves (0–390 V, and -390 to 0 V). Both resonant tanks operate in the half-bridge

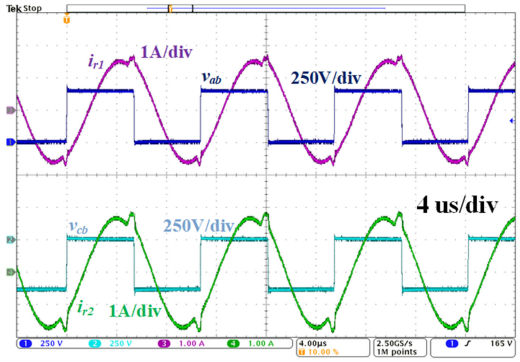

Fig. 15. Steady-state waveforms in mode 3 with $V_o = 222$ V and $P_o = 280$ W.

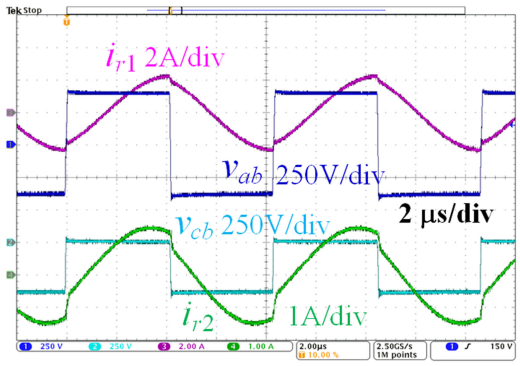

Fig. 16. Steady-state waveforms in mode 4 with $V_o = 280$ V and $P_o = 440$ W.

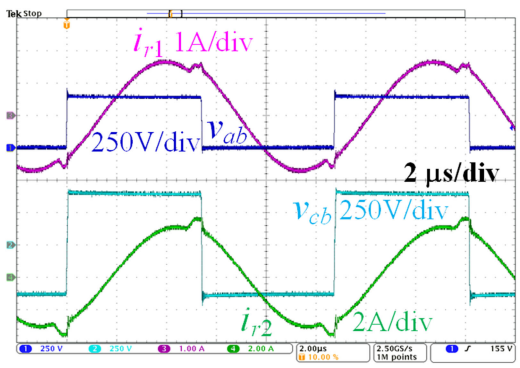

Fig. 17. Steady-state waveforms in mode 5 with $V_o = 354$ V and $P_o = 710$ W.

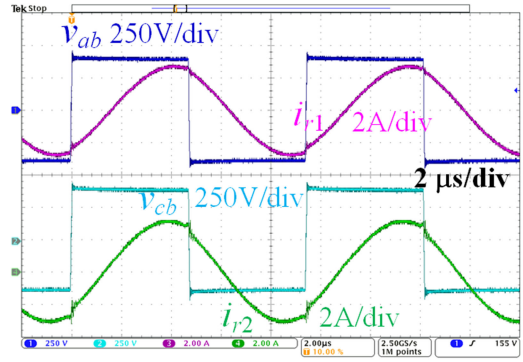

Fig. 18. Steady-state waveforms in mode 6 with $V_o = 420$ V and $P_o = 1000$ W.

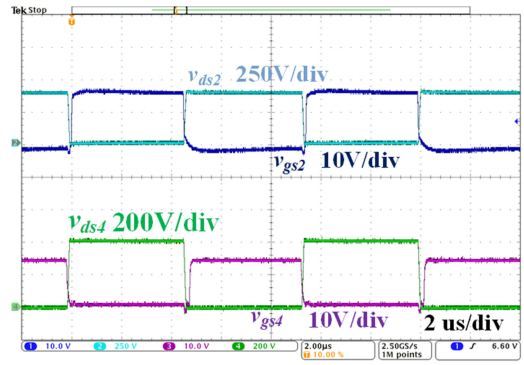

Fig. 19. Steady-state waveforms in mode 1 with $P_o = 100$ W.

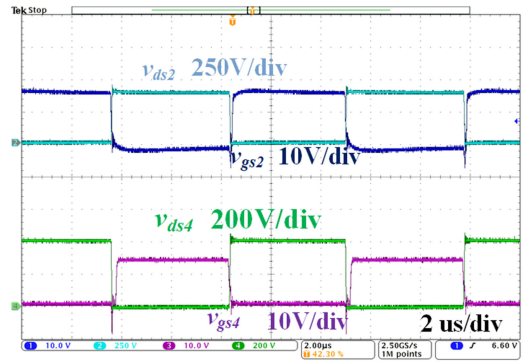

Fig. 20. Steady-state waveforms in mode 4 with $P_o = 500$ W.

mode. Due to the different turns ratios in two transformers, i_{r2} is slightly larger than i_{r1} and RT2 delivers more power than RT1.

The steady-state waveforms in mode 4 are shown in Fig. 16. In this mode, v_{ab} and v_{cb} are both two-level square waves (-390 to 390 V, and -390 to 0 V). RT1 operates in the full-bridge mode, and RT2 operates in the half-bridge mode. Since $v_{ab,\mathrm{rms}}$ is $2v_{cb,\mathrm{rms}}$, RT1 delivers more power than RT2 and i_{r1} is larger than i_{r2}.

The steady-state waveforms in mode 5 are shown in Fig. 17. In this mode, v_{ab} and v_{cb} are both two-level square waves (0–390 V, and -390 to 390 V). RT1 operates in the half-bridge mode, and RT2 operates in the full-bridge mode. In this mode, RT2 delivers more power than RT1 and i_{r2} is larger than i_{r1}.

The steady-state waveforms in mode 6 are shown in Fig. 18. In this mode, v_{ab} and v_{cb} are both two-level square waves (-390 to 390 V, and -390 to 390 V). Both resonant tanks operate in the full-bridge mode. Similarly, due to the different turns ratios, i_{r2} is slightly larger than i_{r1} and RT2 delivers more power than RT1.

The steady-state waveforms at different loads are shown in Figs. 19–21. From the captured v_{ds} and v_{gs}, it can be seen that the primary-side MOSFETs' ZVS are achieved over the entire load range.

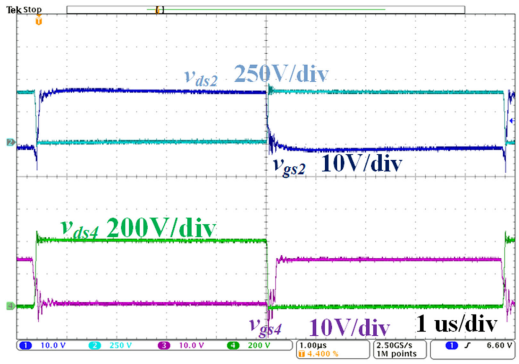

Fig. 21. Steady-state waveforms in mode 6 with $P_o = 1000$ W.

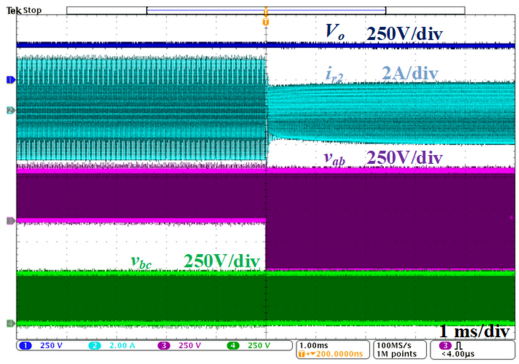

Fig. 22. Transition from mode 3 to mode 4.

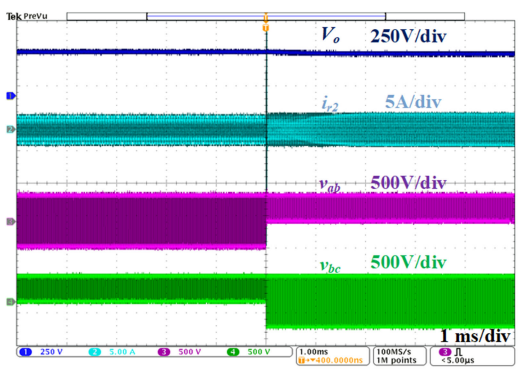

Fig. 23. Transition from mode 4 to mode 5.

The transition waveforms from mode 3 to mode 4, mode 4 to mode 5, and mode 5 to mode 6 are shown in Figs. 22–24, respectively. It can be seen that a general smooth mode transition can be achieved between different adjacent modes.

The measured efficiency data in modes 1–6 with different output voltages are plotted in Figs. 25–30. As shown in the figures, the proposed converter demonstrates 97.05% peak efficiency. An ultrawide output voltage range is achieved. The designed prototype demonstrates good efficiency performance over the ultrawide output voltage range. SiC Schottky diodes (C3D10060A) with zero reverse recovery are employed. Thus, f_s slightly higher than f_r is tolerated, as it improves the overall efficiency over the ultrawide voltage range.

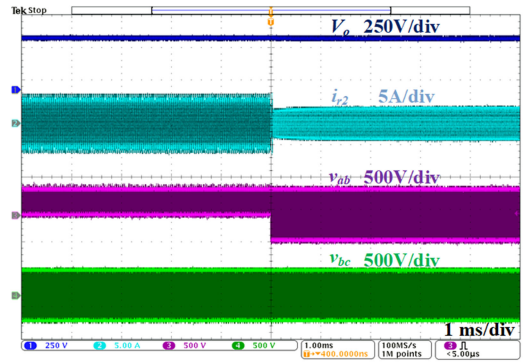

Fig. 24. Transition from mode 5 to mode 6.

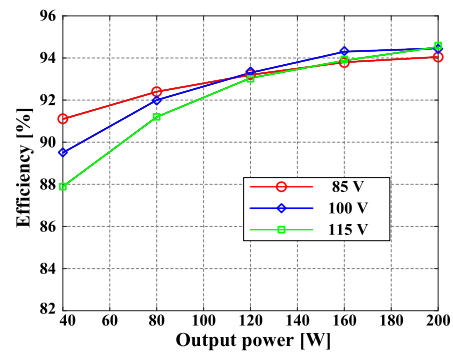

Fig. 25. Measured efficiency curves in mode 1.

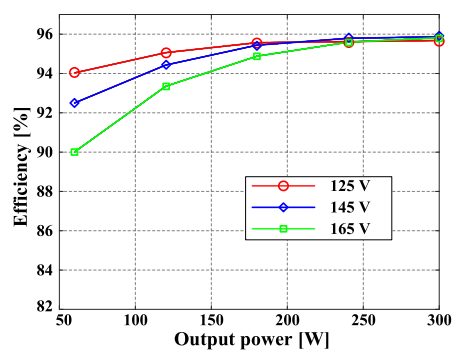

Fig. 26. Measured efficiency curves in mode 2.

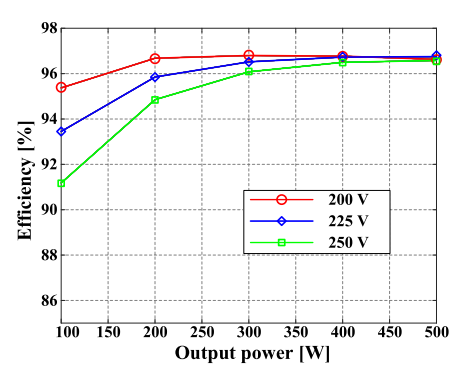

Fig. 27. Measured efficiency curves in mode 3.

TABLE V
COMPARISON WITH EXISTING WIDE OUTPUT VOLTAGE RANGE CONVERTERS

References	*LLC* [30]	Interleaved *LLC* [15]	HB-2*LLC* [24]	SA-VSR [31]	FFPS *LLC* [32]	Proposed
Modulation	PFM	Phase shift + PFM	PFM	PFM + PWM	Phase shift + PFM	PFM
Main control variable	Switching frequency					
Auxiliary control variable	N/A	Phase shift	Mode status	Duty cycle	Phase shift	Mode status
High frequency MOSFETs	4	8	2	6	4	5
Diodes	2	6	4	2	4	4
Control complexity	Low	High	Medium	High	High	Medium
Input voltage (V)	400	390~410	400	390~410	400	390
Output voltage (V)	50~100	150~500	100~420	100~500	120~180	80~450
L_m (μH)	108	430	151.2	400	154	287
Frequency range (kHz)	120~180	45~100	102~236	70~150	100~200	70~130
Peak efficiency	94.5%	98%	95.21%	95.38%	96.5%	97.05%
Rated power	3 kW	3.5 kW	1.5 kW	1.5 kW	3 kW	1 kW

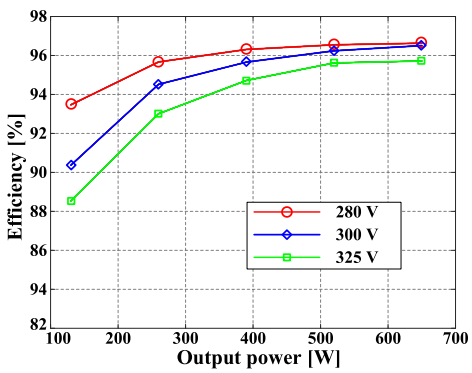

Fig. 28. Measured efficiency curves in mode 4.

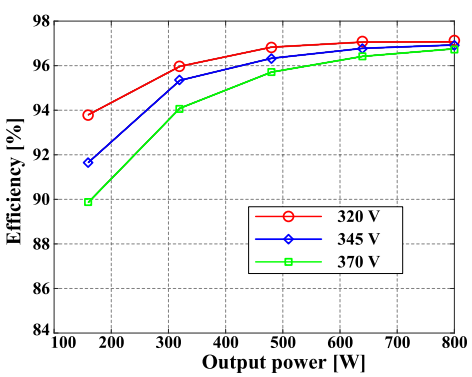

Fig. 29. Measured efficiency curves in mode 5.

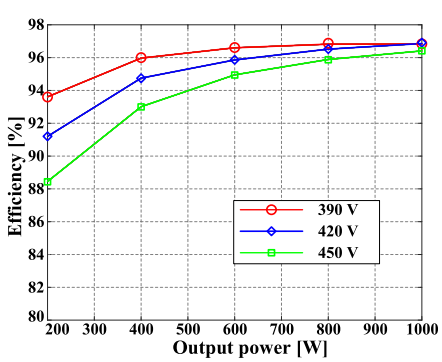

Fig. 30. Measured efficiency curves in mode 6.

A comparison among the proposed topology and some recently reported wide output range topologies is made [15], [24], [30]–[32], and it is summarized in Table V. The proposed topology demonstrates simple pulse-frequency modulation (PFM) modulation, moderate MOSFETs/diodes count, ultrawide output voltage range, narrow frequency band, and good peak efficiency.

VI. CONCLUSION

In this article, a novel H5-bridge-based asymmetric *LLC* resonant converter was proposed. This converter is suitable for wide output voltage applications, including PEV onboard chargers. The H5 inverter bridge was reconfigurable. Therefore, two asymmetric *LLC* resonant tanks could operate in idle, half-bridge, hybrid-bridge, and full-bridge modes. Correspondingly, six modes with a scaled voltage gain profile were obtained. The output voltage range was effectively expanded with moderate L_m and squeezed f_s range. Hence, the drawbacks caused by small L_m and wide f_s range were avoided. The proposed resonant converter's operating principles, circuit modeling, and key design consideration were detailed. The uniqueness of the proposed converter in comparison with the conventional *LLC* resonant converter was analyzed.

To validate the proposed concept, a 1-kW rated prototype with 390 V input and 80–450 V output was built and tested. With 100 kHz f_r, the designed converter had its f_s constrained in the range of 70–130 kHz. The primary-side MOSFETs could achieve ZVS from 10% load to full load. The designed prototype demonstrated 97.05% peak efficiency and good efficiency over the wide output voltage range. The experimental results validate the effectiveness of the proposed converter in wide output voltage range applications.

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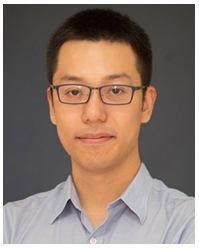

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